

# IR3Y48M

## CCD Signal Process & Digital Interface IC

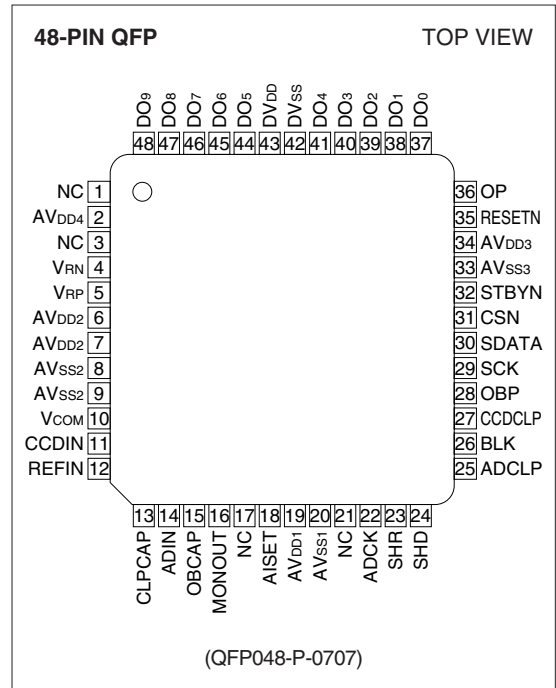
### DESCRIPTION

The IR3Y48M is a CMOS single-chip signal processing IC for CCD area sensors which includes correlated double sampling circuit (CDS), clamp circuit, automatic gain control amplifier (AGC), reference voltage generator, black level detection circuit, 20 MHz 10-bit analog-to-digital converter (ADC), timing circuit for internally required pulses, and serial interface for internal circuits.

### FEATURES

- Low power consumption :  
110 mW (TYP.) at 20 MHz mode
- Wide AGC range : 0 to 36 dB  
(Gain step : 0.094 dB/step)
- High speed sample-and-hold circuits :  
pulse width 10 ns (MIN.)
- Power save operation :  
84 mW (TYP.) at 15 MHz mode
- Standby mode : less than 0.3 mW
- Built-in serial interface
- 10-bit ADC operating up to 20 MHz
  - Non-linearity  
DNL : 0.6 LSB (TYP.)  
INL : 1.5 LSB (TYP.)
- Maximum input level of CCD signals : 1.1 Vp-p
- Accepts a direct signal input to ADC or AGC  
(input level : 1 Vp-p (TYP.))
- Single +3 V power supply
- Package :  
48-pin QFP (QFP048-P-0707) 0.5 mm pin-pitch

### PIN CONNECTIONS





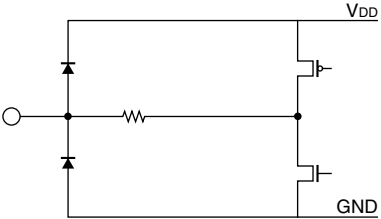
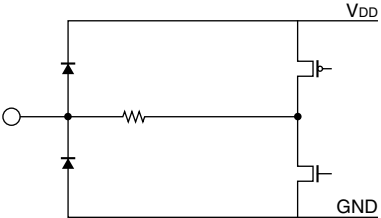
## PIN DESCRIPTION

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
1	NC	—		No connection.
2	AVDD4	—		Supply of 2.7 to 3.6 V analog power.
3	NC	—		No connection.
4	VRN	O		ADC internal negative reference voltage. (Connect to AVss via 0.1 $\mu$ F.)
5	VRP	O		ADC internal positive reference voltage. (Connect to AVss via 0.1 $\mu$ F.)
6	AVDD2	—		Supply of 2.7 to 3.6 V analog power.
7	AVDD2	—		Supply of 2.7 to 3.6 V analog power.
8	AVSS2	—		An analog grounding pin.
9	AVSS2	—		An analog grounding pin.
10	VCOM	O		ADC internal common reference voltage. (Connect to AVss via 0.1 $\mu$ F.)
11	CCDIN	I		CDS circuit data input.
12	REFIN	I		CDS circuit reference input.
13	CLPCAP	O		Clamp level output. (Connect to AVss via 0.1 $\mu$ F.)
14	ADIN	I		ADIN signal input.
15	OBCAP	O		Black level integration voltage. (Connect to AVss via 0.033 $\mu$ F.)
16	MONOUT	O		Monitor output of CDS or AGC.

※ Internal gate

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
17	NC	—		No connection.
18	AISSET	I		Internal analog circuit bias input. (Connect to AVSS via 4.7 kΩ.)
19	AVDD1	—		Supply of 2.7 to 3.6 V analog power.
20	AVSS1	—		An analog grounding pin.
21	NC	—		No connection.
22	ADCK	I		ADC sampling clock input.
23	SHR	I		Reference sampling pulse input.
24	SHD	I		Data sampling pulse input.
25	ADCLP	I		Clamp and black calibration control for ADIN signal.
26	BLK	I		Blanking pulse input.
27	CCDCLP	I		Clamp control input.
28	OBP	I		Black level period pulse input.
29	SCK	I		Serial port clock input.
30	SDATA	I		Serial port data input.
31	CSN	I		Serial port chip selection (active at low).
32	STBYN	I	Standby control (standby at low).	
33	AVSS3	—		An analog grounding pin.
34	AVDD3	—		Supply of 2.7 to 3.6 V analog power.
35	RESETN	I		Reset signal input (reset at low).
36	OP	I		Serial I/F operation code enable pin (active at low).

※ Internal gate

PIN NO.	SYMBOL	I/O	EQUIVALENT CIRCUIT	DESCRIPTION
37	DO <sub>0</sub>	O		ADC digital output (LSB). (Capable of High-Z)
38	DO <sub>1</sub>	O		ADC digital output. (Capable of High-Z)
39	DO <sub>2</sub>	O		ADC digital output. (Capable of High-Z)
40	DO <sub>3</sub>	O		ADC digital output. (Capable of High-Z)
41	DO <sub>4</sub>	O		ADC digital output. (Capable of High-Z)
42	DV <sub>SS</sub>	-		Digital output driver GND. A digital grounding pin.
43	DV <sub>DD</sub>	-		Digital output driver power supply. (2.7 to 3.6 V)
44	DO <sub>5</sub>	O		ADC digital output. (Capable of High-Z)
45	DO <sub>6</sub>	O		ADC digital output. (Capable of High-Z)
46	DO <sub>7</sub>	O		ADC digital output. (Capable of High-Z)
47	DO <sub>8</sub>	O		ADC digital output. (Capable of High-Z)
48	DO <sub>9</sub>	O		ADC digital output (MSB). (Capable of High-Z)

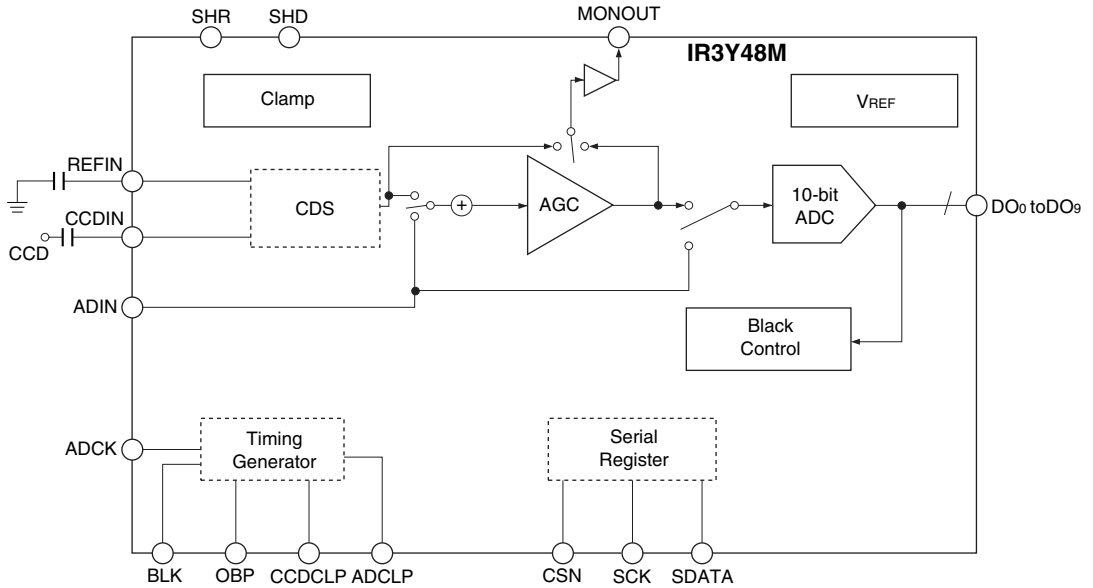
**NOTES :**

- NC pins are recommended to be connected to AV<sub>SS</sub> on PCB even they are not connected electrically in the chip.
- High-Z at standby.

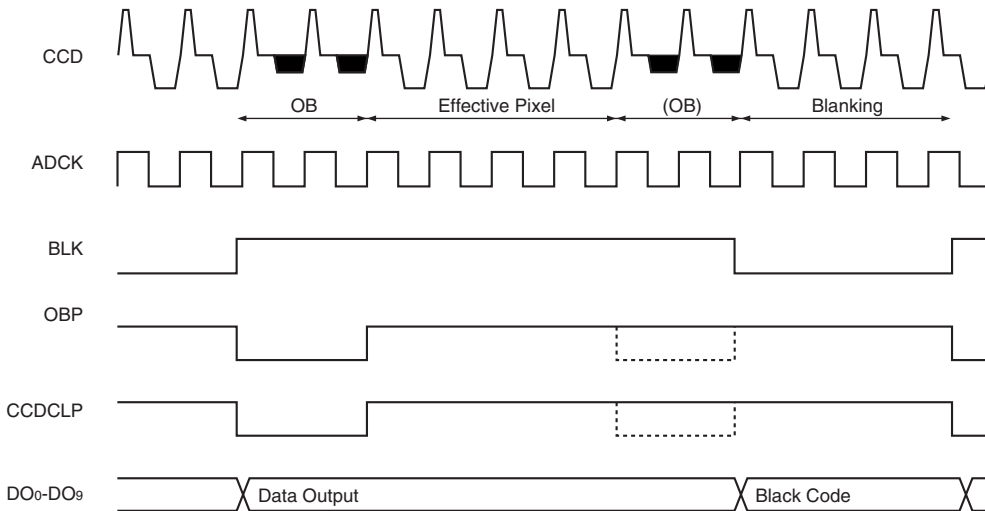
## FUNCTIONAL DESCRIPTION

### Outline

The configuration of IR3Y48M is described below.



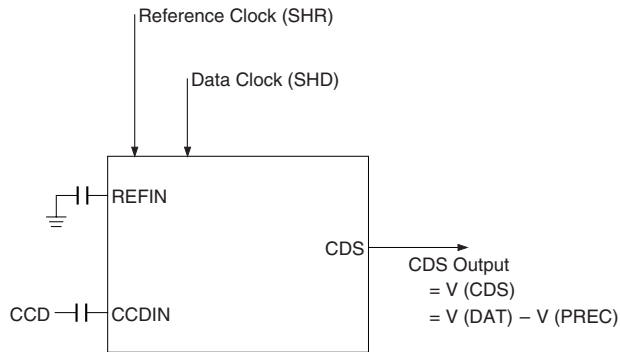
### GENERAL TIMING



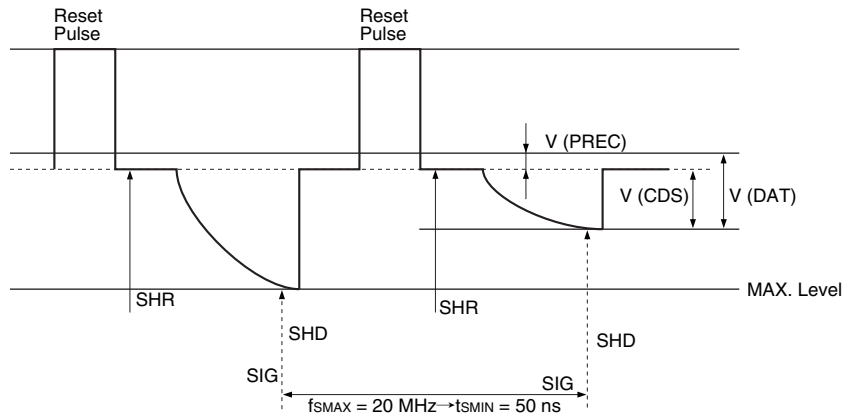
### CDS Circuit

CDS circuit holds CCD precharge (reference) level at SHR pulse, then it samples CCD pixel data at SHD pulse. Correlated (common) noise is removed by subtraction of precharge level from pixel data level.

CDS has the gain of maximum 12 dB (6 dB/step). This gain is a part of total gain and it is controlled by register value similar to gain in AGC circuit. Connect signal from CCD sensor to CCDIN pin through C-coupling. Place the same capacitor between REFIN and AVss.



CDS Operation

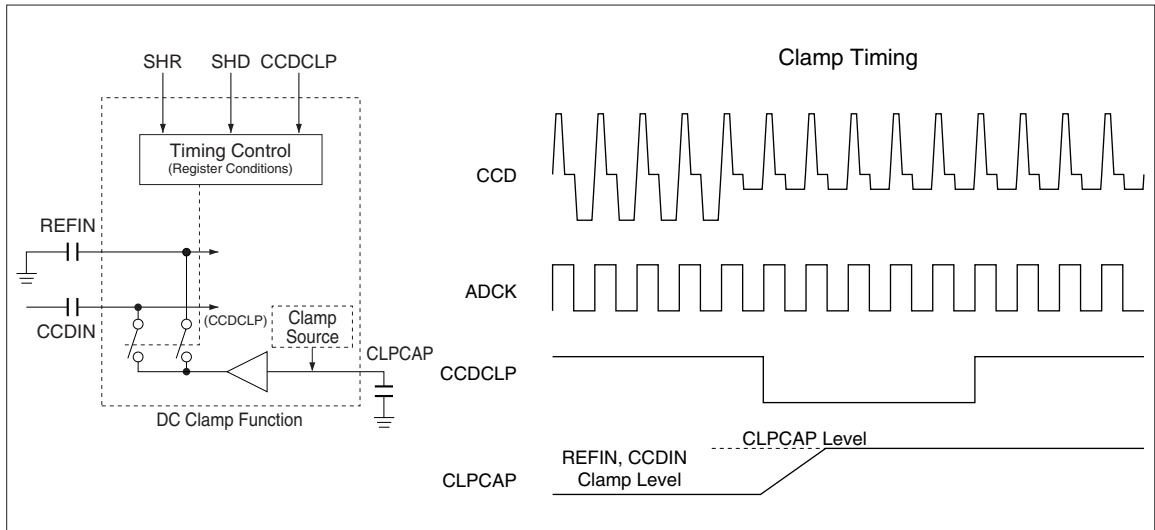


## Clamp Circuit

### DC CLAMP

DC level of the analog input is fixed by internal DC clamp circuit. DC level of C-coupled CCD signal at CDS input is set to CLPCAP by DC clamping.

Normally clamp switch is turned on at black level calibration period. Place 0.1  $\mu\text{F}$  external capacitance between CLPCAP and AVss.



### CLAMP OF ADIN SIGNAL

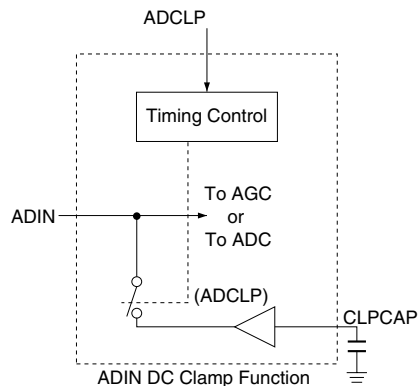
Clamp operation for ADIN path is also available. Note that clamp voltage [CLPCAP] is different between CCD input and ADIN.

ADCLP signal is used for both clamp and black level control at ADIN input mode. It is also possible to turn off clamp operation by register setting.

### CLAMP CONTROL

Following items are selectable through register setting.

- Clamp current  
Normal or fast clamp is selectable for charge current. (Select normal clamp in general)
- Clamp target  
Input signal (REFIN and CCDIN) to be clamped is selectable. It is also possible to turn off the clamp function.





### Black Level Cancel Circuit

The purpose of black level cancel is to adjust the AGC input level which can equalize the ADC output code to black level code written in the register. The black level cancelling is generally done during OBP (optical black period) pulsed by OBP pulse. The register value ((1 to 16 to 127 LSB : default 64 LSB) is written by serial interface.

Black level cancel loop is established while OBP is low (when pulse is not inverted).

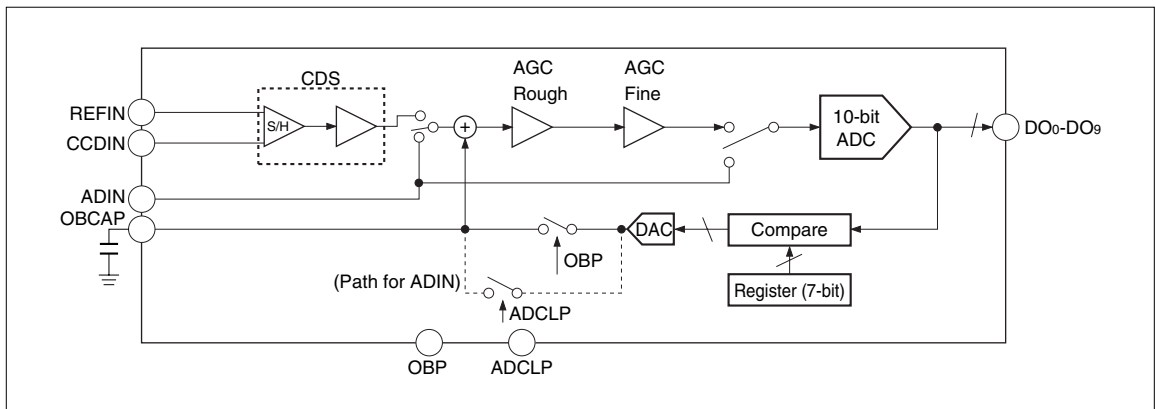
In this loop, ADC output code is compared with register setting. During OB period, the OBP voltage gradually terminates into certain voltage resulting the output code equal to the register setting.

The OBP voltage is discharged under following status :

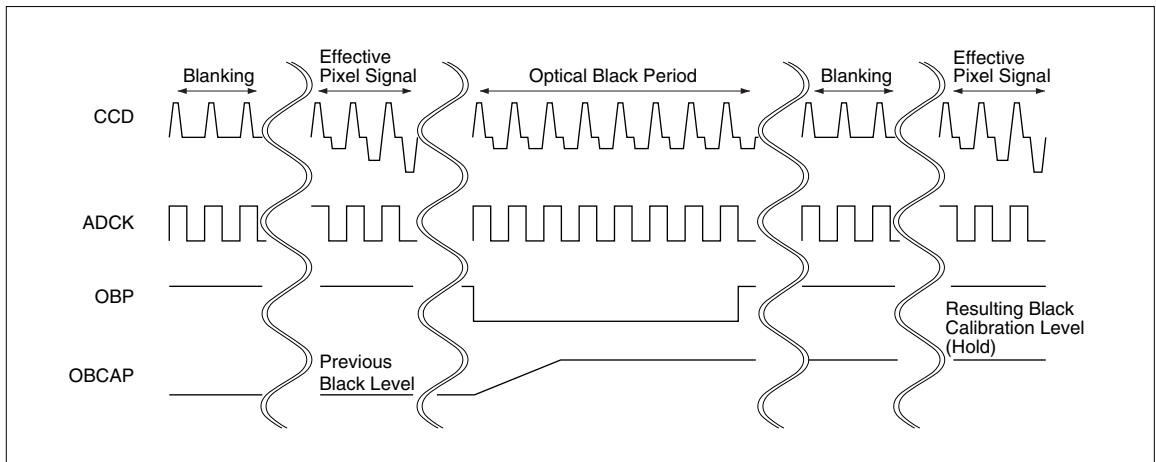
- ① Set black level reset register to 1
- ② Set RESET pin low
- ③ Power down (by STBYN or register control)

The period to reach the final value depends on the status of chip. It may take more than one thousand pixels at start-up or after reset. It may take only several pixels when the status is not changed. DC clamp [CCDCLP] is allowed during OBP low.

Black level cancelling for ADIN signal (broken line in the chart) is controlled by ADCLP pulse (clamp and OB control are done simultaneously) instead of OBP.



**Black Level Calibration**



**Black Level Calibration Timing**

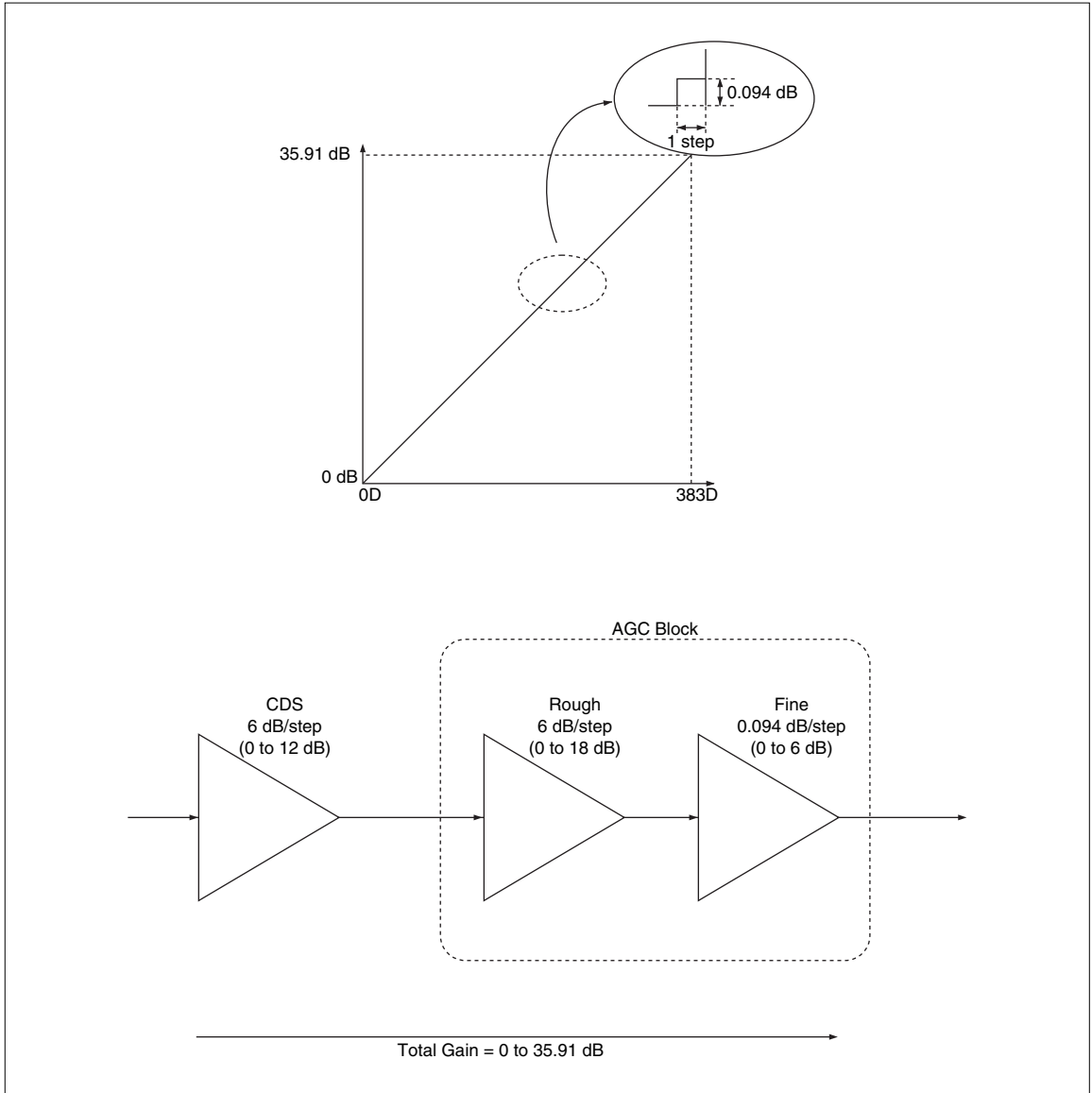
### Gain Control Circuit

The total gain for CCD input signal covers from 0 to 36 dB.

This range consists of CDS (0 to 12 dB (6 dB/step)), AGC rough (0 to 18 dB (6 dB/step)), and AGC fine (0 to 6 dB (0.094 dB/step)). Total gain is

controlled (as described below) by 9-bit gain control register. The gain is fixed to maximum gain when the code exceeds 382 (decimal).

The gain of ADIN (which bypassing CDS) is 0 to 24 dB.



Gain Control

## A/D Converter Circuit

IR3Y48M integrates 20 MHz 10-bit full pipeline A/D converter (ADC).

## A/D CONVERSION RANGE

The analog input range of the ADC is determined by VREF circuit integrated in IR3Y48M. At ADC direct input (ADIN) mode (Mode (1) Register D<sub>5</sub> = 1), feed 1 V<sub>p-p</sub> (full scale) signal based on clamp level as zero reference into ADIN input pin.

## A/D CONVERTER OUTPUT CODE (AT MODE (1) REGISTER D<sub>5</sub> = 1)

The digital output format is binary.

Thus, "all zero" digital output with zero reference input (ADIN = CLPCAP), "all one" digital output with full-scale input (ADIN = CLPCAP + 1 V (TYP.)).

## CLOCK, PIPELINE DELAY AND OUTPUT DIGITAL DATA TIMING

The A/D conversion is performed based on the clock fed to ADCK pin.

The track-and-hold operation is completed at falling (when not inverted) edge of ADCK.

The 10-bit width parallel data is obtained at rising edge after 5.5 clock pipeline delay. (Sampling edge is selectable by register setting.)

## CODE AT CLAMP LEVEL

### (AT MODE (1) REGISTER D<sub>5</sub> = 0, D<sub>4</sub> = 1)

The output code at clamp level can be set throughout (1 to) 16 to 127 LSB at the step of 1 LSB by register setting.

## ADC OUTPUT CODE LOGIC

ADC digital output is High-Z under following conditions :

- ① Set ADC output register to 1
- ② Set SYBYN pin low
- ③ Power down (by STBYN or register control)

## DIGITAL OUTPUT CODE

According to ADIN, digital codes are determined as follows :

**Data Output at Straight Binary  
[Mode (1) Register D<sub>2</sub> = 0, D<sub>5</sub> = 1]**

ADIN	DIGITAL CODE									
	MSB									LSB
	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
Clamp reference + 1 V	1	1	1	1	1	1	1	1	1	1
:					:					
:	1	0	0	0	0	0	0	0	0	0
:	0	1	1	1	1	1	1	1	1	1
:					:					
Clamp reference	0	0	0	0	0	0	0	0	0	0

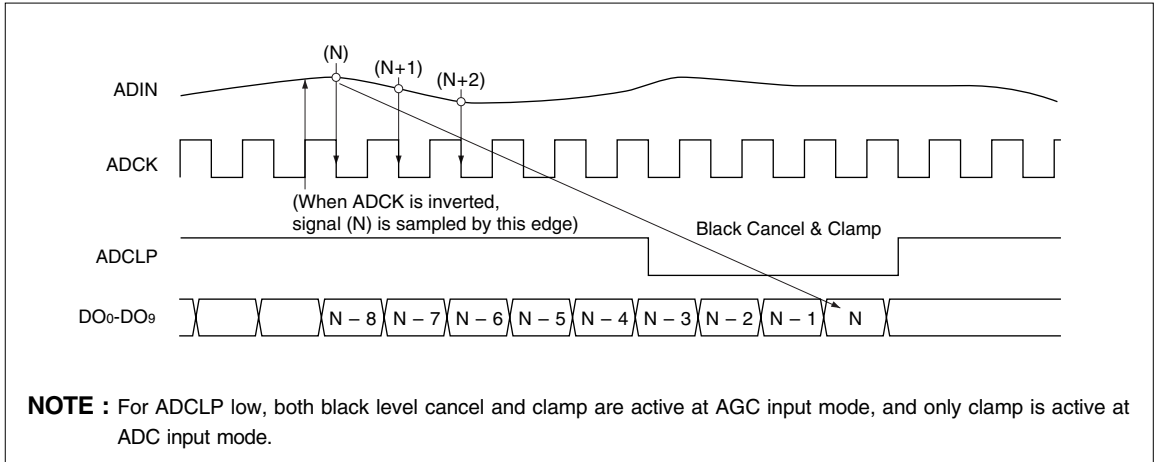
**Other Functions**

**ADC DIRECT INPUT (ADIN MODE)**

Direct input path to ADC or AGC is realized by register setting. This direct path can be turned off by register. Black level cancel and clamp are performed at the same timing of ADCLP low.

These controls can be masked by register setting. BLK, SHR, and SHD controls are ignored at ADIN mode.

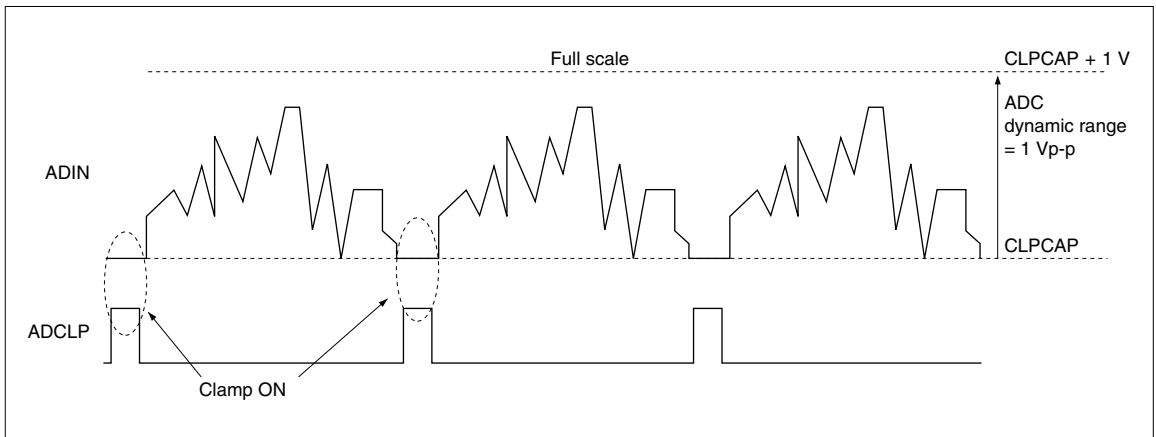
The signal at AGC input is shown below.



**ADIN Signal Processing (AGC Input)**

Operation at ADC direct input is shown below. The zero reference (CLPCAP) is established by

ADCLP pulse. The ADIN input range is from CLPCAP + 1 V (TYP.) (full scale).



**ADIN Signal Input Level**

**STANDBY MODE**

The standby mode can be set either by register setting or STBYN pin.

If one of the above is set, IR3Y48M powers down. ("OR" logic)

## MONITOR OUTPUT

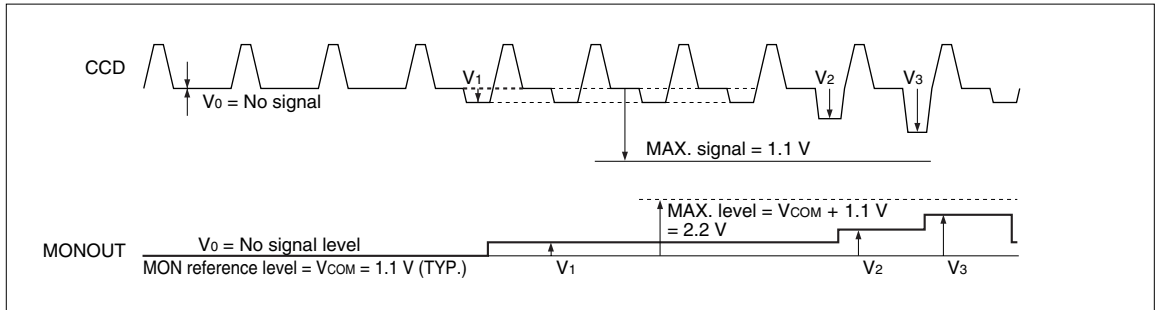
By setting the register, the signal from MONOUT is selectable. Alternatives are OFF, CDS output, AGC output, or REFIN/CCDIN output. Even at the CDS gain is set to a certain gain, the CDS output on MONOUT is multiplied by  $1/\text{gain}$  resulting the level before CDS amplification.

The output level of MONOUT is shown below. The

MONOUT level is  $V_{COM}$  (1.1 V, TYP.) at zero reference level. For the maximum amplitude (1.1 Vp-p), the output level is 2.2 V (TYP.).

### CAUTION :

$V_{COM}$  pin does not have enough driving capabilities.



Monitor Output Level

## POLARITY INVERSION

Following timing pulse of IR3Y48M control can be inverted by register setting :

- ① ADCK (A/D converter sampling pulse)
- ② SHR, SHD (CDS sampling clock)
- ③ BLK, OBP, CCDCLP, ADCLP (Enable controls)

## POWER SAVE

Power save mode is selectable for the sampling frequency below 15 MHz.

The power consumption at this mode is lower than 20 MHz mode.

## General Notice for Power Supply

It is recommended to supply both  $AV_{DD}$  and  $DV_{DD}$  supply from single regulator.

(Observe absolute maximum rating specification :  $DV_{DD} \leq (AV_{DD} + 0.3 \text{ V})$  even at the power-up and power-down sequence.)

Refer to "**APPLICATION CIRCUIT EXAMPLE**" against noise of power supply.

## Serial Interface Circuit

The internal registers of IR3Y48M are controlled through 3-wire serial interface.

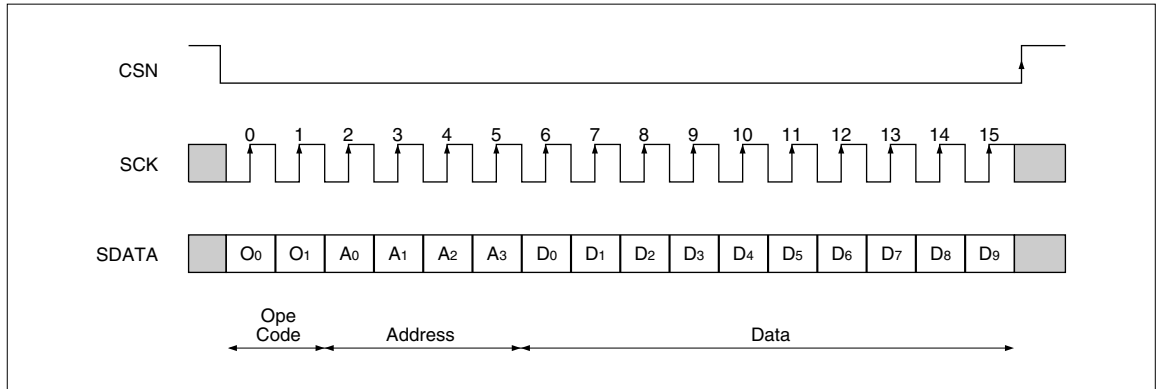
The 16-bit length control data consists of 2-bit operation code, 4-bit address, and 10-bit data. The controller should set each bit synchronizing to SCK falling since IR3Y48M (receiver) acquire data at SCK rising edge. The data is valid while CSN is low.

The written data comes effective at rising edge of CSN.

Fix CSN to high when no access is conducted.

It is forbidden to write data to the address that is not listed.

Always give 16 times SCK rising during CSN low. All data are ignored when SCK rising during CSN low is less than 16.



**Serial Write Control**

The effect of operation code is determined by OP pin control.

When OP pin is high, the data are always valid regardless of O0 and O1.

When OP pin is low, operation code control is active, and the data is written only when both O0 = 0 and O1 = 1 are true.

## Registers

IR3Y48M has 10-bit x 5 registers to control its operations.

All registers are write only. The serial registers are written by serial interface.

### Register Map

R/W	ADDRESS				REFERENCE NAME	MAJOR FUNCTIONS [DATA]
	A3	A2	A1	A0		
W	0	0	0	0	Mode (1)	ADCK polarity/ADIN connection/Frequency mode/ADC output/Black level reset/Standby
W	0	0	0	1	Mode (2)	Clamp current/ADIN clamp/Clamp target/S/H, enable logic/Monitor selection
W	0	0	1	0	Gain	Total gain
W	0	0	1	1	Black level	ADC code at black level (1 LSB step)
W	0	1	0	0	Test register	Test mode (ADIN coupling mode)

1. Reference name                      Mode (1)

2. Register address  
[Write]

A3	A2	A1	A0
0	0	0	0

3. Register bit assignment

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	X	X	X	0	0	0	0	0	0	0
Functions										
ADCK polarity				<->						
ADIN connection					<---->					
Frequency mode							<->			
ADC output								<->		
Black level reset									<->	
Standby										<->

X : Don't care

## 4. Register operations

	CONTROLS											OPERATIONS	NOTE
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
ADCK polarity				0								Normal operation as timing chart	
				1								ADCK clock inversion	
ADIN connection				0	0							ADIN function OFF	
				0	1							ADIN signal to AGC	
				1	X							ADIN signal to ADC	
Frequency mode							0					20 MHz mode	
							1					15 MHz mode	
ADC output								0				Normal operation [ADC data output]	
								1				ADC output High-Z [or logic of STBYN]	1
Black level reset									0			Normal operation	
										1		Black level reset [or logic of RESETN]	2
Standby										0		Normal operation	
											1	Standby [or logic of STBYN]	

**NOTES :**

X : Don't care

- ADC output is set to high impedance if one of following case is true.
  - Case 1 : Set "ADC output" bit to "1".
  - Case 2 : Set STBYN pin to low.
  - Case 3 : Set "Standby" bit to "1".
- Black level integral CAP [OBCAP] is discharged if following case is true.
  - Case 1 : Set "Black level reset" to "1".
  - Case 2 : Set RESETN pin to low.



1. Reference name Mode (2)

2. Register address

[Write]

A3	A2	A1	A0
0	0	0	1

3. Register bit assignment

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	X	X	0	0	0	0	0	0	0	0
Functions										
Clamp current			<->							
ADIN clamp				<->						
Clamp target					<---->					
S/H, enable logic							<---->			
Monitor selection									<---->	

X : Don't care

4. Register operations

	CONTROLS										OPERATIONS	NOTE	
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0			
Clamp current			0									Normal clamp	
			1									Fast clamp	
ADIN clamp				0								Clamp operation active for ADIN	
				1								No clamp for ADIN	
Clamp target					0	0						Normal mode [clamp both REFIN & CCDIN]	
					0	1						Clamp REFIN only	
					1	0						Clamp CCDIN only	
					1	1						Clamp OFF	
S/H, enable logic							0	0				Normal operation as timing chart	
							0	1				S/H control polarity inversion	1
							1	0				Enable control polarity inversion	2
							1	1				Both of S/H and enable inversion	
Monitor selection									0	0		Monitor OFF	
									0	1		CDS signal to monitor	3
									1	0		AGC output monitor	4
									1	1		Output REFIN and CCDIN (for calibration)	

**NOTES :**

1. The S/H signals are SHR and SHD.
2. The enable controls are BLK, OBP, CCDCLP, and ADCLP.
3. At this mode, monitor output gain = 0 dB regardless of CDS gain.
4. At this mode, monitor output depends on CDS gain.

1. Reference name Gain

2. Register address  
[Write]

A3	A2	A1	A0
0	0	1	0

3. Register bit assignment

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	X	0	0	0	0	0	0	0	0	0
Functions										
Total gain	←----->									

X : Don't care

4. Register operations

	CONTROLS										DECIMAL	HEX	TOTAL GAIN (dB)	NOTE	
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0					
Total gain (For CCDIN input)	0	0	0	0	0	0	0	0	0	0	0	0	0.000		
	0	0	0	0	0	0	0	0	0	1	1	1	0.094		
	0	0	0	0	0	0	0	0	1	0	2	2	0.188		
	0	0	0	0	0	0	0	0	1	1	3	3	0.281		
	0	0	0	0	0	0	0	1	0	0	4	4	0.375		
		...													
	0	0	0	1	1	1	1	1	1	0	62	3E	5.813		
	0	0	0	1	1	1	1	1	1	1	63	3F	5.906		
	0	0	1	0	0	0	0	0	0	0	64	40	6.000		
	0	0	1	0	0	0	0	0	0	1	65	41	6.094		
		...													
	0	1	0	0	0	0	0	0	0	0	128	80	12.000		
		...													
	0	1	1	0	0	0	0	0	0	0	192	C0	18.000		
		...													
	1	0	0	0	0	0	0	0	0	0	256	100	24.000		
		...													
	1	0	1	0	0	0	0	0	0	0	320	140	30.000		
		...													
	1	0	1	1	1	1	1	1	0	0	380	17C	35.625		
1	0	1	1	1	1	1	1	0	1	381	17D	35.719			
1	0	1	1	1	1	1	1	1	0	382	17E	35.813			
1	0	1	1	1	1	1	1	1	1	383	17F	35.906			
1	1	0	0	0	0	0	0	0	0	384	180	35.906			
	...														
1	1	1	1	1	1	1	1	1	1	511	1FF	35.906	1		

	CONTROLS										DECIMAL	HEX	TOTAL GAIN (dB)	NOTE
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0				
Total gain (For AGC input)	0	0	0	0	0	0	0	0	0	0	0	0	0.000	
	0	0	0	0	0	0	0	0	0	1	1	1	0.094	
	0	0	0	0	0	0	0	0	1	0	2	2	0.188	
	0	0	0	0	0	0	0	0	1	1	3	3	0.281	
	0	0	0	0	0	0	0	1	0	0	4	4	0.375	
				...										
	0	0	0	1	1	1	1	1	1	0	62	3E	5.813	
	0	0	0	1	1	1	1	1	1	1	63	3F	5.906	
	0	0	1	0	0	0	0	0	0	0	64	40	6.000	
	0	0	1	0	0	0	0	0	0	1	65	41	6.094	
				...										
	0	1	0	0	0	0	0	0	0	0	128	80	12.000	
				...										
	0	1	1	0	0	0	0	0	0	0	192	C0	18.000	
				...										
	0	1	1	1	1	1	1	1	1	0	254	FE	23.813	
	0	1	1	1	1	1	1	1	1	1	255	FF	23.906	
	1	0	0	0	0	0	0	0	0	0	256	100	23.906	
	1	0	0	0	0	0	0	0	0	1	257	101	23.906	
	1	0	0	0	0	0	0	0	1	0	258	102	23.906	
			...										2	
1	1	1	1	1	1	1	1	1	1	511	1FF	23.906		

**NOTES :**

- Gain is always (35.90625 dB, TYP.) for code greater than 382 (decimal).
- Gain is always (23.906 dB, TYP.) for code greater than 254 (decimal).

1. Reference name            Black level

2. Register address  
[Write]

A3	A2	A1	A0
0	0	1	1

3. Register bit assignment

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	X	X	X	1	0	0	0	0	0	0
Functions										
Black level				←-----→						

X : Don't care

4. Register operations

	OPERATIONS [ADC CODE : BINARY]										DECIMAL	HEX	NOTE	
	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0				
Black level				0	0	0	0	0	0	0		FORBIDDEN	FORBIDDEN	
				0	0	0	0	0	0	1		1	1	1
												...		1
				0	0	0	1	1	1	1		15	F	1
				0	0	1	0	0	0	0		16	10	
				0	0	1	0	0	0	1		17	11	
				0	0	1	0	0	1	0		18	12	
				0	0	1	0	0	1	1		19	13	
												...		
				0	1	0	0	0	0	0		32	20	
												...		
				1	0	0	0	0	0	0		64	40	
												...		
				1	1	1	1	1	0	0		124	7C	
				1	1	1	1	1	0	1		125	7D	
			1	1	1	1	1	1	0		126	7E		
			1	1	1	1	1	1	1		127	7F		

**NOTE :**

- Codes 1 to 15 are available but not recommended black calibration period is specified under 15 < code < 128.

1. Reference name                      Test register

2. Register address  
[Write]

A3	A2	A1	A0
0	1	0	0

3. Register bit assignment

	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Default	X	X	X	0	0	0	0	0	0	0
Functions										
ADIN test mode				<->						

X : Don't care

4. Register operations

	CONTROLS										OPERATIONS
	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
ADIN test mode				0							Normal operation
				1							VCOM centered ADIN for AC coupling

**NOTE :**

D5 to D0 must always be "0".

Test register (D6) is prepared for ADIN AC coupled input. Using this mode the signal center is set to VCOM. No clamp signals are required at this mode.

Connect C-coupled output to ADIN. The resistance 50 kΩ between ADIN (14 pin) and CLPCAP (13 pin) stabilize the DC level at ADIN pin.

**ABSOLUTE MAXIMUM RATINGS** (AVSS = DVSS = 0 V, all voltages are with respect to GND.)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT	NOTE
Power supply voltage	AVDD		-0.3 to +4.5	V	
	DVDD		-0.3 to +4.5 or AVDD + 0.3	V	1
Voltage difference	VDLT	DVDD – AVDD	0.3	V	
Input current	IIN	Except PS	±10	mA	
Analog input voltage	VINA		AVSS – 0.3 to AVDD + 0.3	V	
Digital input voltage (Input pin)	VINL		AVSS – 0.3 to AVDD + 0.3	V	
Digital input voltage (Output pin)	VONL		AVSS – 0.3 to AVDD + 0.3	V	2
Operating temperature	TOPR		-30 to +85	°C	
Storage temperature	TSTG		-40 to +125	°C	

**NOTES :**

1. The higher voltage of 4.5 V and AVDD + 0.3 V specifies maximum value of DVDD absolute maximum rating.
2. The VONL limits the excess voltage applied to digital output pins.

**WARNING :**

Operation at or beyond these limits may result in permanent damage to the device. Normal operating specifications are not guaranteed at these extremes.

**RECOMMENDED OPERATING CONDITIONS**

(AVSS = DVSS = 0 V, all voltages are with respect to GND.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage	Analog	At start-up, turn on AVDD before (or at the same time as) turning on DVDD.	2.7	3.0	3.6	V
	Digital output		2.7	3.0	AVDD	V

**ELECTRICAL CHARACTERISTICS****Supply Current**

(TA = +25 °C, AVDD = DVDD = 3.0 V)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply current at normal operation	Analog	fs = 15 MHz (At 15 MHz mode)		28	34	mA	1
	Digital			3	6	mA	
	Analog	fs = 20 MHz (At 20 MHz mode)		36	44	mA	
	Digital			3.5	7	mA	
Supply current at monitor active	IPE	(At 20 MHz mode)		38	46	mA	
Supply current at power down	IPD				0.1	mA	2

**NOTES :**

1. Specified under monitor function off.
2. Measured under no analog input and clock fixed at low.

## Analog Specifications

(Unless otherwise specified,  $V_{DD} = DV_{DD} = 3.0\text{ V}$ ,  $T_A = +25\text{ }^\circ\text{C}$ , signal frequency  $f_{IN} = 1\text{ MHz}$ , signal level =  $-1\text{ dB}$  (full scale))

The current direction flowing into the pin is positive direction.

### CDS & CLAMP CIRCUITS

(Sampling frequency  $f_s = 20\text{ MHz}$ )

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Analog input range	$V_{ICDS}$	Normally		1.1		Vp-p	1
	$V_{IAI}$	At ADIN		1.1		Vp-p	
Input referred noise	NI	At $f_s = 20\text{ MHz}$	At gain = max.	100		$\mu\text{V}_{\text{rms}}$	2
			At gain = min.	400		$\mu\text{V}_{\text{rms}}$	
Input capacitance	$C_{IN}$	CCDIN, ADIN & REFIN		15		pF	
Input Bandwidth	CBW				1	pixel	3
Clamp voltage	$V_{CLPCAP}$	Normally	1.65	1.8	1.95	V	
		At ADIN	1.15	1.3	1.45	V	
Black calibration period	tBKCAL				2000	pixel	4, 5

### NOTES :

- Normally : Signal path through CDS→AGC→ADC  
In this case analog input range is downward from clamp voltage.  
ADIN : Signal bypassing CDS (Direct AGC or ADC input)  
In this case analog input range is upward from clamp voltage.

- Specified at MONOUT pin. The noise bandwidth is 100 kHz to 5 MHz.
- Bandwidth from CCDIN/REFIN to ADC. The bandwidth is specified as the settling time of ADC output for step input (full scale – 1 dB) response (at gain = min.).
- Black calibration period is the period of stabilization of output code within  $\pm 1\text{ LSB}$  (average) compared to register value for the black level code of 0 to 50% of the full scale input. (Assuming external capacitance =  $0.033\text{ }\mu\text{F}$ .)

External capacitor value to OBCAP pin determines the bandwidth of the black level cancel loop. Since the gain of the loop depends on sampling frequency, the maximum frequency (settling within certain pixels) and the minimum frequency (avoiding oscillation of the circuit) are defined.

- Select the external capacitor referring the following list based on the minimum and maximum operating frequencies.

If the black level settling specification (within 2 000 pixels) could be ignored, the maximum sampling frequency for  $0.1\text{ }\mu\text{F}$  and  $0.33\text{ }\mu\text{F}$  will extend according to the increment.

PARAMETER	MODE	OBCAP	MIN.	MAX.	UNIT
Available sampling frequency	20 MHz mode	$0.033\text{ }\mu\text{F}$	7.6	20	MHz
	15 MHz mode	$0.033\text{ }\mu\text{F}$	5.8	15	MHz
		$0.1\text{ }\mu\text{F}$	2.2	5.7	MHz
		$0.33\text{ }\mu\text{F}$	0.6	1.7	MHz

**TOTAL GAIN**

PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
At normal operation	Min. gain	GMNN	Gain between REFIN/CCDIN and MONOUT	-1.9	-0.9	0.1	dB	1
	Max. gain	GMXN		34.906	35.906	36.906	dB	
	Gain step	GST		0	0.094	0.188	dB	
At ADIN operation	Min. gain	GMNNA	Gain between ADIN and MONOUT	-1.3	-0.3	0.7	dB	1
	Max. gain	GMXNA		22.906	23.906	24.906	dB	
	Gain step	GSTA		0	0.094	0.188	dB	
CDS and AGC total gain relative accuracy		ERPA				±1	LSB	2

**NOTES :**

- Gain is specified for gain between AGC input and MONOUT output.
- Gain measured at MONOUT pin.

**A/D CONVERTER CIRCUIT**

(fs = 20 MHz. Signal is given to ADIN.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Resolution	RES				10	bits	
Integral non-linearity	INL	fs = 20 MHz (At 20 MHz mode)		±1.5	±2.5	LSB	
Differential non-linearity	DNL	fs = 15 MHz (At 15 MHz mode)		±0.5	±1.0	LSB	
S/N	SN			58		dB	
S/ (N+D)	SND			56		dB	
ADC common voltage	VCOM		1.0	1.1	1.2	V	
VREF voltage (positive)	VRP		1.25	1.35	1.45	V	
VREF voltage (negative)	VRN		0.75	0.85	0.95	V	
ADC output black level calibration code	CCAL		16		127	LSB	1
Black level step	STCAL			1		LSB	

**NOTE :**

- Black level calibration period (t<sub>BKCAL</sub>) is specified for code = 16 to 127 LSB.  
Although black level code of 1 to 15 could be set, t<sub>BKCAL</sub> is not guaranteed for these codes.



## Switching Characteristics

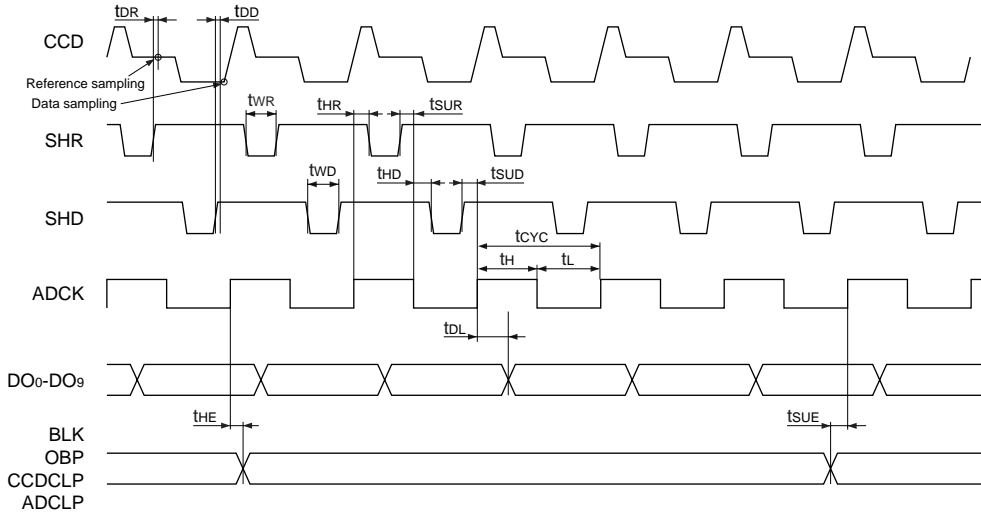
(AVDD, DVDD = 2.7 to 3.6 V, AVSS, DVSS = 0 V, TOPR = -30 to +85 °C, CL < 10 pF)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Conversion speed	fs		0.5		20	MHz	
Clock cycle period	tcyc		50			ns	
Clock rise time	tR	(30%→70%) AVDD, DVDD			2	ns	
Clock fall time	tF	(70%→30%) AVDD, DVDD			2	ns	
Clock low period	tL		23			ns	
Clock high period	tH		23			ns	
Min. reference pulse	tWR		10			ns	
Min. data pulse	tWD		10			ns	
Reference sampling delay	tDR				4	ns	
Data sampling delay	tDD				4	ns	
Reference pulse setup	tSUR		-3			ns	1
Data pulse setup	tSUD		-3			ns	2
Reference pulse hold	tHR		5			ns	
Data pulse hold	tHD		5			ns	
Enable pulse setup	tsue		10			ns	
Enable pulse hold	the		10			ns	
Tristate disable delay	tDLD	Active→High-Z		20		ns	
Tristate enable delay	tDLE	High-Z→Active		20		ns	
ADC output data delay	tDL1		2			ns	
	tDL2				35	ns	

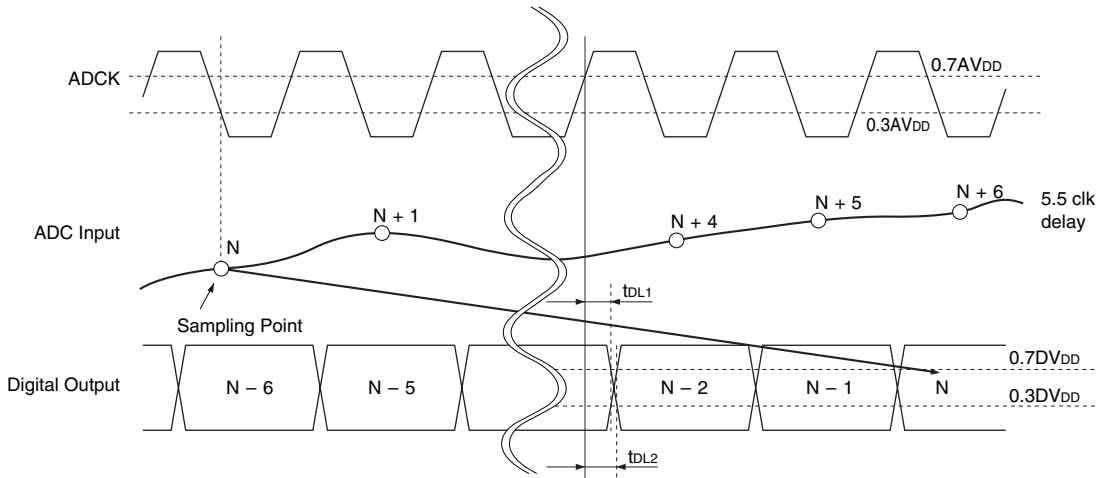
### NOTES :

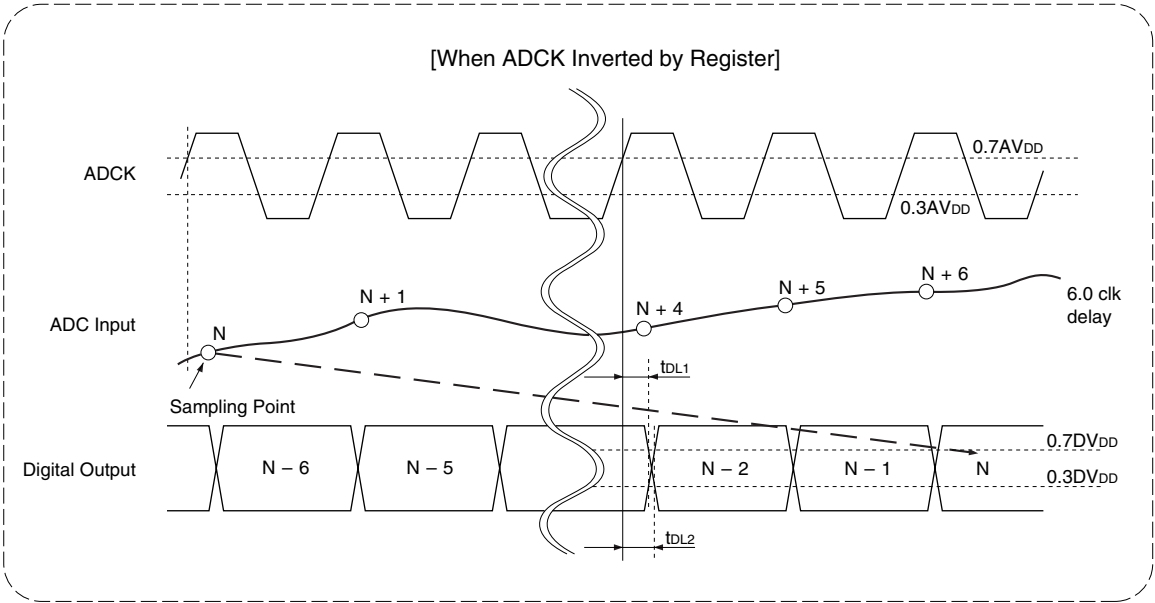
- When SHR ↑ is earlier than ADCK ↓, assumed positive.  
(In the above table, SHR ↑ can be delayed a maximum of 3 ns behind ADCK ↓.)
- When SHD ↑ is earlier than ADCK ↑, assumed positive.  
(In the above table, SHD ↑ can be delayed a maximum of 3 ns behind ADCK ↑.)

TIMING CHART



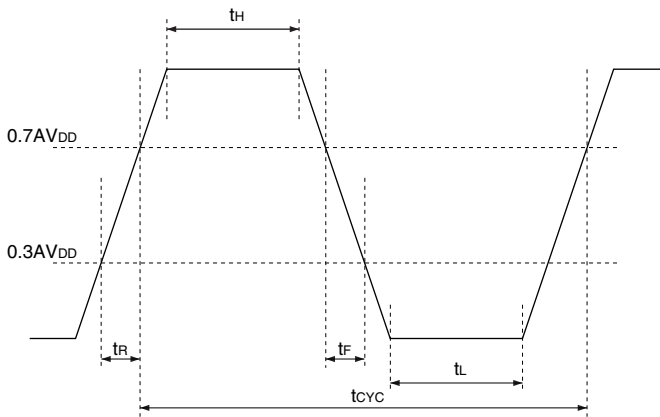
ADIN : ADC Direct Input





**NOTE :** At default condition of ADIN mode, falling edge of sampling and rising edge of data out are selected. If each edge should be a rising edge, invert the ADCK by register setting. (The figure shown on the previous page is the default, the following is the inverted one.)

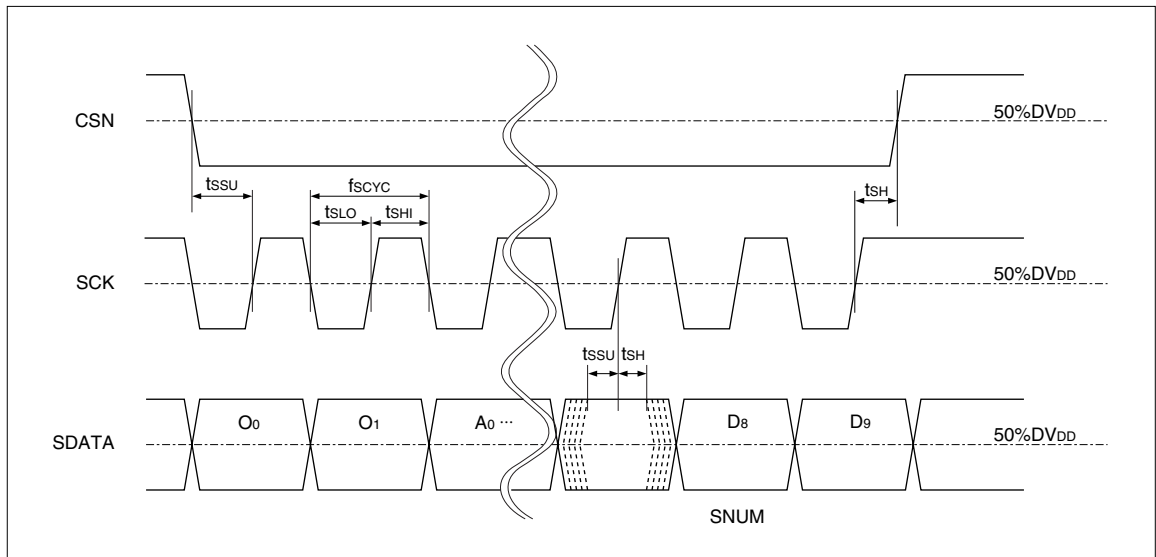
Clock Waveform



## CONTROL INTERFACE TIMING

(AVDD, DVDD = 2.7 to 3.6 V, AVSS, DVSS = 0 V, TOPR = -30 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SCK clock cycle time	fscyc				10	MHz
SCK clock low width	tsLO		40			ns
SCK clock high width	tSHI		40			ns
Setup time	tssU		20			ns
Hold time	tSH		20			ns
SCK, CSN rise time	tsR	30% → 70%			6	ns
SCK, CSN fall time	tsF	70% → 30%			6	ns
Serial data number	SNUM			16		pcs



Serial I/F Timing

## Digital DC Characteristics

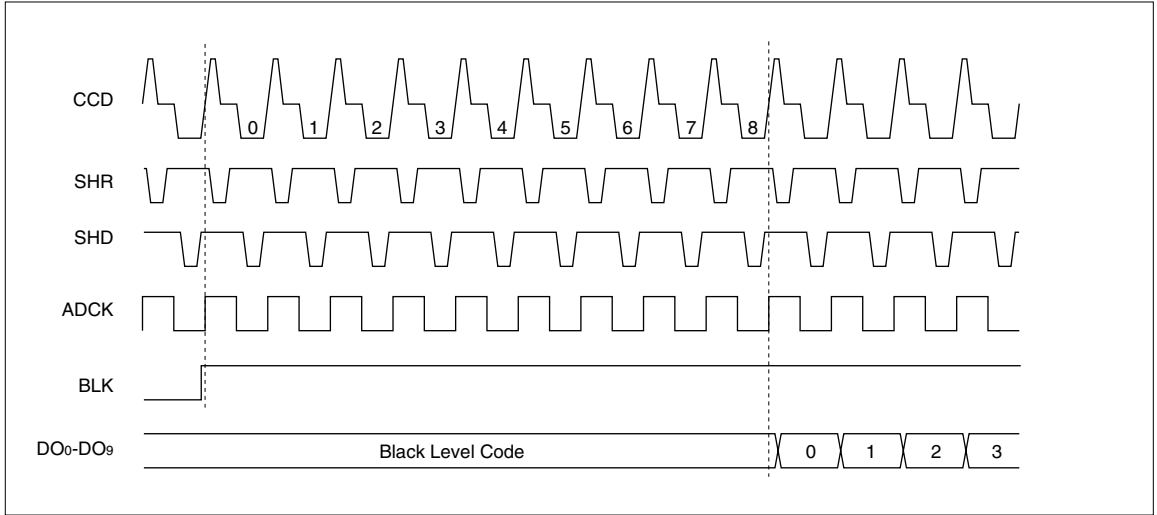
(AVDD, DVDD = 2.7 to 3.6 V, AVSS, DVSS = 0 V, TOPR = -30 to +85 °C, measured as DC characteristics.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	VIL1				0.3AVDD	V	1
Input "High" voltage	VIH1		0.7AVDD			V	
Output "Low" voltage	VOL	IOI = 1 mA			0.3DVDD	V	
Output "High" voltage	VOH	IOH = -1 mA	0.7DVDD			V	
"High" leakage current	ILING				±10	μA	
High-Z leakage current	IOZ				±10	μA	

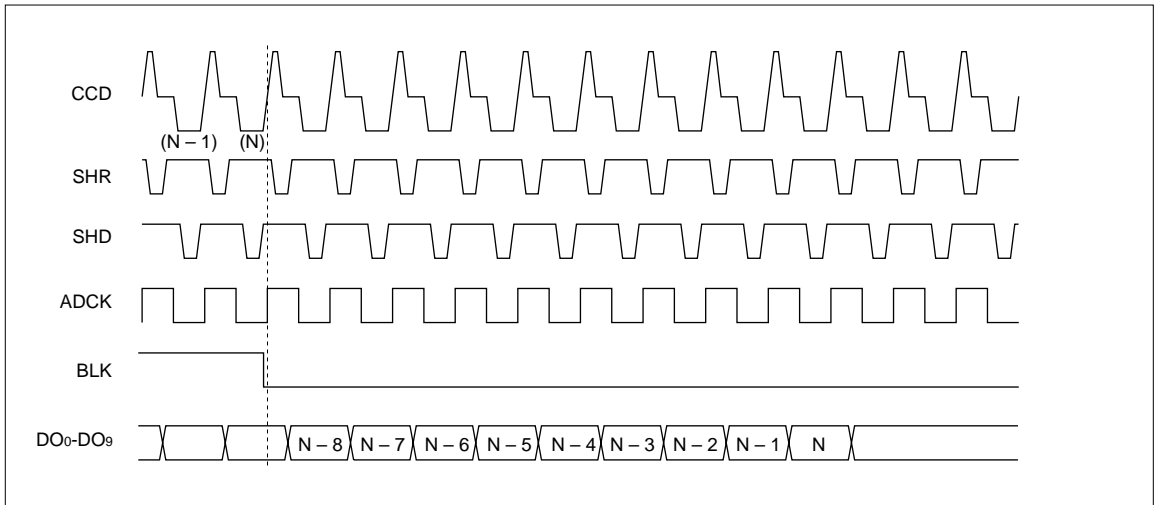
## NOTE :

- Specified for SHD, SHR, ADCK, BLK, OBP, CCDCLP, ADCLP, CSN, SCK, SDATA, RESETN, STBYN, and OP.

### Data Output Sequence



**Pixel Data Readout Sequence (1) : Conversion Start**

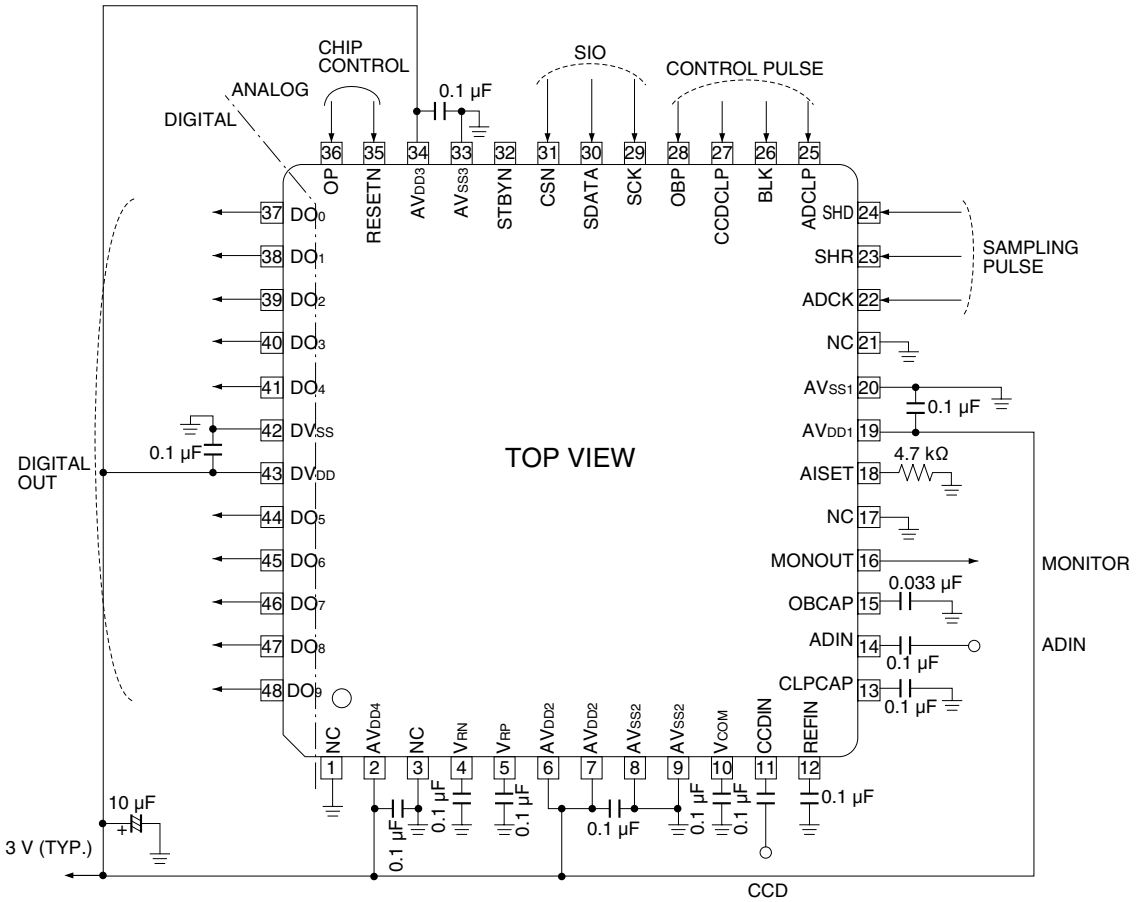


**Pixel Data Readout Sequence (2) : Conversion End**

### APPLICATION CIRCUIT EXAMPLE

The following schematic is the reference circuit for system design.

Optimize capacitance and resistance according to the system environment.



## PACKAGE

(Unit : mm)

## 48 QFP (QFP048-P-0707)

