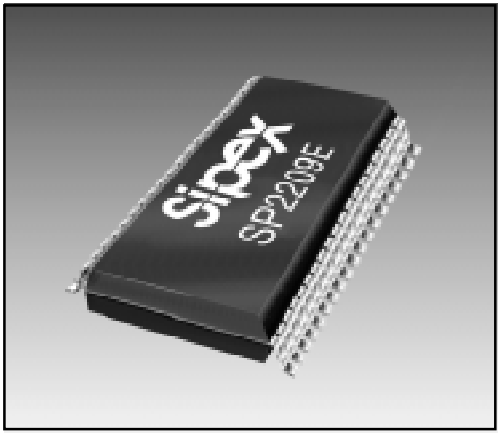
High ESD Dual Port RS-232 Transceiver

- Meets True EIA/TIA-232-F Standards
- Complies with 89/336/EEC EMC Directive
- Single +12V Power Supply
- <5mA Low Power CMOS Operation
- 100µA Low Standby Current
- Operates With +3V Or +5V Logic
- Allows +3.3V to +5V Standby Supply
- Two Complete Serial Ports, 6 Drivers and 10 Receivers
- One Receiver On Each Port Active In Standby
- Failsafe Receiver Outputs
- 460kbps Minimum Data Rate
- Guaranteed LapLink® - Compatible
- Ideal For High Speed RS-232 Applications
- 0.1µF Charge Pump Capacitors
- Low EMI Emissions (EN55022)
- Pin Compatible To ADM2209E device
- Enhanced ESD Specifications:
  ±15KV Human Body Model
  ±15KV EN61000-4-2 Air Discharge
  ±8KV EN61000-4-2 Contact Discharge
- Fast Transient Burst (EFT) Immunity (EN61000-4-2)



DESCRIPTION

The rugged, high ESD **SP2209E** device is a complete dual RS-232 port integrated onto a single integrated circuit. Six drivers and ten receivers provide designers a dual port solution fully meeting the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in applications such as personal desktop computers and workstations. Features include high transmission rates, low power consumption, an internal charge-pump power supply that requires only two capacitors, space saving 38-pin TSSOP package dimensions, and compatibility with the EU directive on electromagnetic compatibility. This device is ideal for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged. This device is also immune to high RF field strengths without special shielding precautions.

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{DD}.....-0.3V to +14.0V
V_{STBY}.....-0.3V to +7V

Input Voltages
T_XINA.....-0.3V to (V_{STBY} + 0.3V)
T_XINB.....-0.3V to (V_{STBY} + 0.3V)
R_XINA.....±15V
R_XINB.....±15V

Output Voltages
T_XOUTA.....±15V
T_XOUTB.....±15V
R_XOUTA.....-0.3V to (V_{STBY} + 0.3V)
R_XOUTB.....-0.3V to (V_{STBY} + 0.3V)

Short-Circuit Duration
T_XOUTA.....Continuous
T_XOUTB.....Continuous

Storage Temperature.....-65°C to +150°C

Power Dissipation per package
38-pin TSSOP (derate 14.3mW/ºC above +70ºC).....1200mW

SPECIFICATIONS

Unless otherwise noted, the following specifications apply for V_{DD} = +12.0V ± 10%, V_{STBY} = +3.3V ± 5% or +5V ± 10%, C1 = C2 = 0.1µF, and T_{AMB} = T_{MIN} to T_{MAX}.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DC CHARACTERISTICS					
Supply Current			5	mA	no load, all driver inputs at 0.4V or 2.1V, all receiver inputs at +15V or -15V
Standby Supply Current, V_{STBY}		100	200	µA	no load, all driver inputs at V_{STBY} or open
CMOS LOGIC INPUTS AND RECEIVER OUTPUTS					
Input Logic Threshold Voltage LOW HIGH	 2.1		 0.4	 V	T_{AMB} = 25ºC
Input Leakage Current		10	25	µA	Driver input at 0V
Output Voltage LOW		0.2	0.4	V	I_{OL} = +1.6mA
Output Voltage HIGH	2.4			V	I_{OH} = -40µA
Output Leakage Current		±0.05	±5	µA	V_{DD} = 0V, (except R_5OUTA and R_5OUTB)

SPECIFICATIONS (continued)

Unless otherwise noted, the following specifications apply for V_{DD} = +12.0V ± 10%, V_{STBY} = +3.3V ± 5% or +5V ± 10%, C1 = C2 = 0.1µF, and T_{AMB} = T_{MIN} to T_{MAX}.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER OUTPUTS					
Output Voltage Swing	±5.0	±9.0		V	all driver outputs loaded with 3KΩ to GND
Output Resistance	300			Ω	V_{DD} = V_{STBY} = 0V, V_{OUT} = ±2V
Output Short-Circuit Current	±5	±15	±30	mA	one driver output shorted, V_{IN} = 0.8V, V_{OUT} = 0V
RECEIVER INPUTS					
Input Voltage Range	-15		+15	V	
Input Threshold LOW	0.4	1.45		V	
Input Threshold HIGH		1.7	2.4	V	
Input Hysteresis		0.25		V	
Input Resistance	3	5	7	kΩ	V_{IN} = ±15V
TIMING CHARACTERISTICS					
Driver Maximum Data Rate	460 460 920			kbps	R_L = 3kΩ to 7kΩ, C_L = 50pF to 470pF R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF T_{AMB} = 0°C to +85°C, V_{STBY} = 5V ± 10% only R_L = 3kΩ to 7kΩ, C_L = 50pF to 470pF, V_{STBY} = 5V ± 5%, V_{DD} = 12V + 5%
Driver Propagation Delay t_{PHL} t_{PLH}		 1.0 1.0		 µs	 R_L = 3kΩ, C_L = 1000pF, refer to *Figures 3* and *5* R_L = 3kΩ, C_L = 1000pF, refer to *Figures 3* and *5*
Driver Transition-Region Slew Rate	6 4	16 16		V/µs	R_L = 3kΩ to 7kΩ, C_L = 50pF to 470pF R_L = 3kΩ to 7kΩ, C_L = 50pF to 1000pF V_{STBY} = 5V ± 10% only, measurements taken from -3.0V to +3.0V or +3.0V to -3.0V
Receiver Maximum Data Rate	460 920			kbps	C_L = 150pF C_L = 150pF, V_{STBY} = 5V + 5% only
Receiver Propagation Delay t_{PHL} (R1x - R4x) t_{PLH} (R1x -R4x) t_{PHL} (R5x) t_{PLH} (R5x)		 0.4 0.4 1.0 1.0	 0.75 0.75 2.0 2.0	 µs	 C_L = 150pF, refer to *Figures 4* and *6* C_L = 150pF, refer to *Figures 4* and *6* C_L = 150pF, refer to *Figures 4* and *6* C_L = 150pF, refer to *Figures 4* and *6*
Receiver Output Rise Time		30		ns	refer to *Figures 4 and 6*
Receiver Output Fall Time		30		ns	refer to *Figures 4 and 6*
OPERATING CHARACTERISTICS					
Operating Voltage Range, V_{DD}	+10.8	+12.0	+13.2	V	
Standby Voltage Range, V_{STBY}	+3.15		+5.5	V	
Operating Temperature, T_{AMB}	-40		+85	°C	

NAME	FUNCTION	PIN NUMBER
R_5OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A.	1
R_4OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A.	2
R_3OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A.	3
R_2OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A.	4
R_1OUTA	+3.3V to +5V TTL/CMOS logic level receiver output for port A.	5
T_3INA	+3.3V to +5V TTL/CMOS logic level driver input for port A.	6
T_2INA	+3.3V to +5V TTL/CMOS logic level driver input for port A.	7
T_1INA	+3.3V to +5V TTL/CMOS logic level driver input for port A.	8
STBY	+3.3V to +5V standby power supply for receivers R_5OUTA and R_5OUTB.	9
V_{DD}	+12V power supply	10
C+	Positive terminal for the polarized C1 charge-pump capacitor.	11
T_1INB	+3.3V to +5V TTL/CMOS logic level driver input for port B.	12
T_2INB	+3.3V to +5V TTL/CMOS logic level driver input for port B.	13
T_3INB	+3.3V to +5V TTL/CMOS logic level driver input for port B.	14
R_1OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B.	15
R_2OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B.	16
R_3OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B.	17
R_4OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B.	18
R_5OUTB	+3.3V to +5V TTL/CMOS logic level receiver output for port B.	19
R_5INB	RS-232 receiver input for port B.	20
R_4INB	RS-232 receiver input for port B.	21
R_3INB	RS-232 receiver input for port B.	22
R_2INB	RS-232 receiver input for port B.	23
R_1INB	RS-232 receiver input for port B.	24
T_3OUTB	RS-232 driver output for port B.	25
T_2OUTB	RS-232 driver output for port B.	26
T_1OUTB	RS-232 driver output for port B.	27
GND	Ground.	28
C-	Negative terminal for the polarized C1 charge-pump capacitor.	29
V-	-12V output generated by the charge pump at the negative terminal of the polarized C2 charge-pump capacitor.	30

Table 1. Device Pin Description

NAME	FUNCTION	PIN NUMBER
T_1OUTA	RS-232 driver output for port A.	31
T_2OUTA	RS-232 driver output for port A.	32
T_3OUTA	RS-232 driver output for port A.	33
R_1INA	RS-232 receiver input for port A.	34
R_2INA	RS-232 receiver input for port A.	35
R_3INA	RS-232 receiver input for port A.	36
R_4INA	RS-232 receiver input for port A.	37
R_5INA	RS-232 receiver input for port A.	38

Table 1. Device Pin Description (continued)

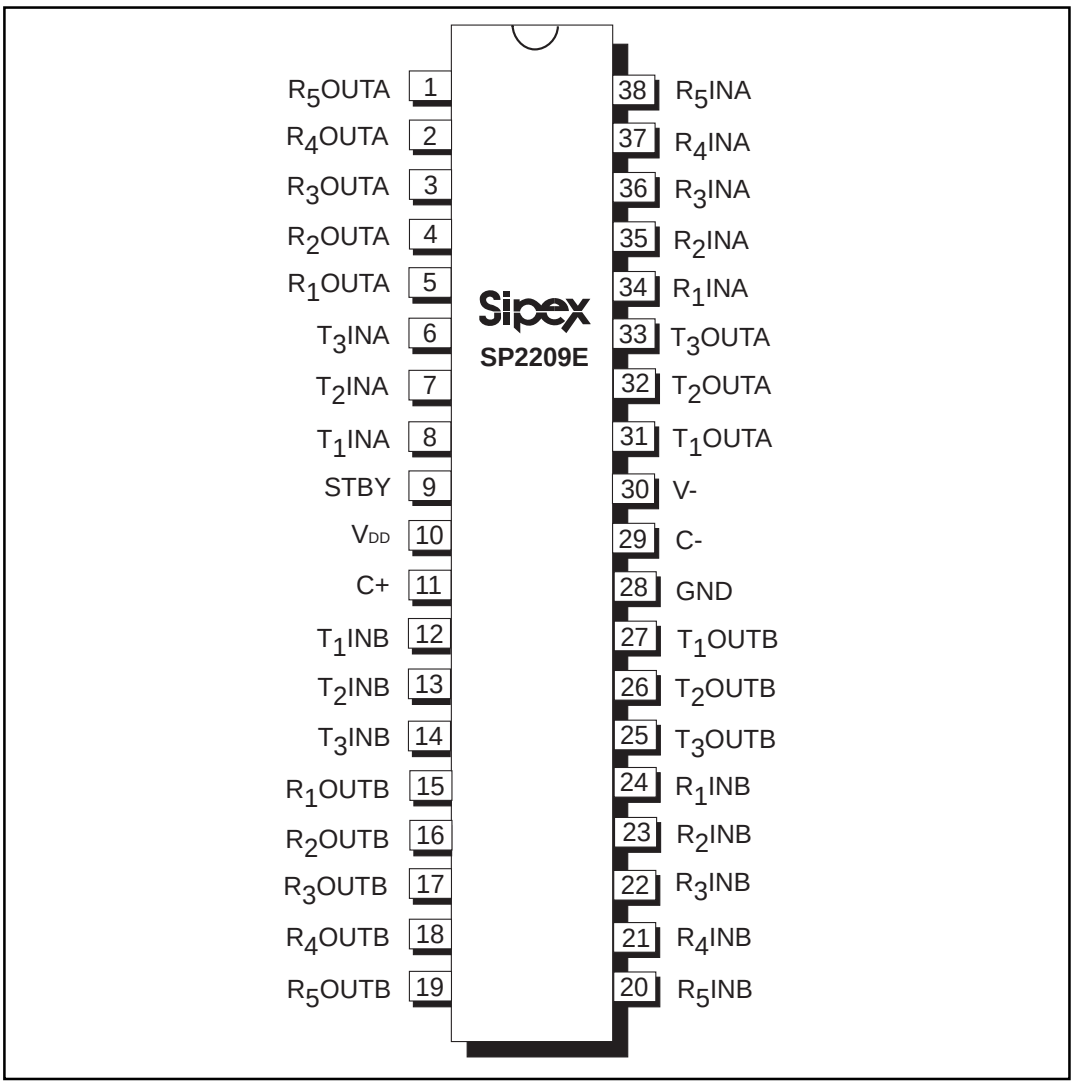


Figure 1. SP2209E Pinout Configuration

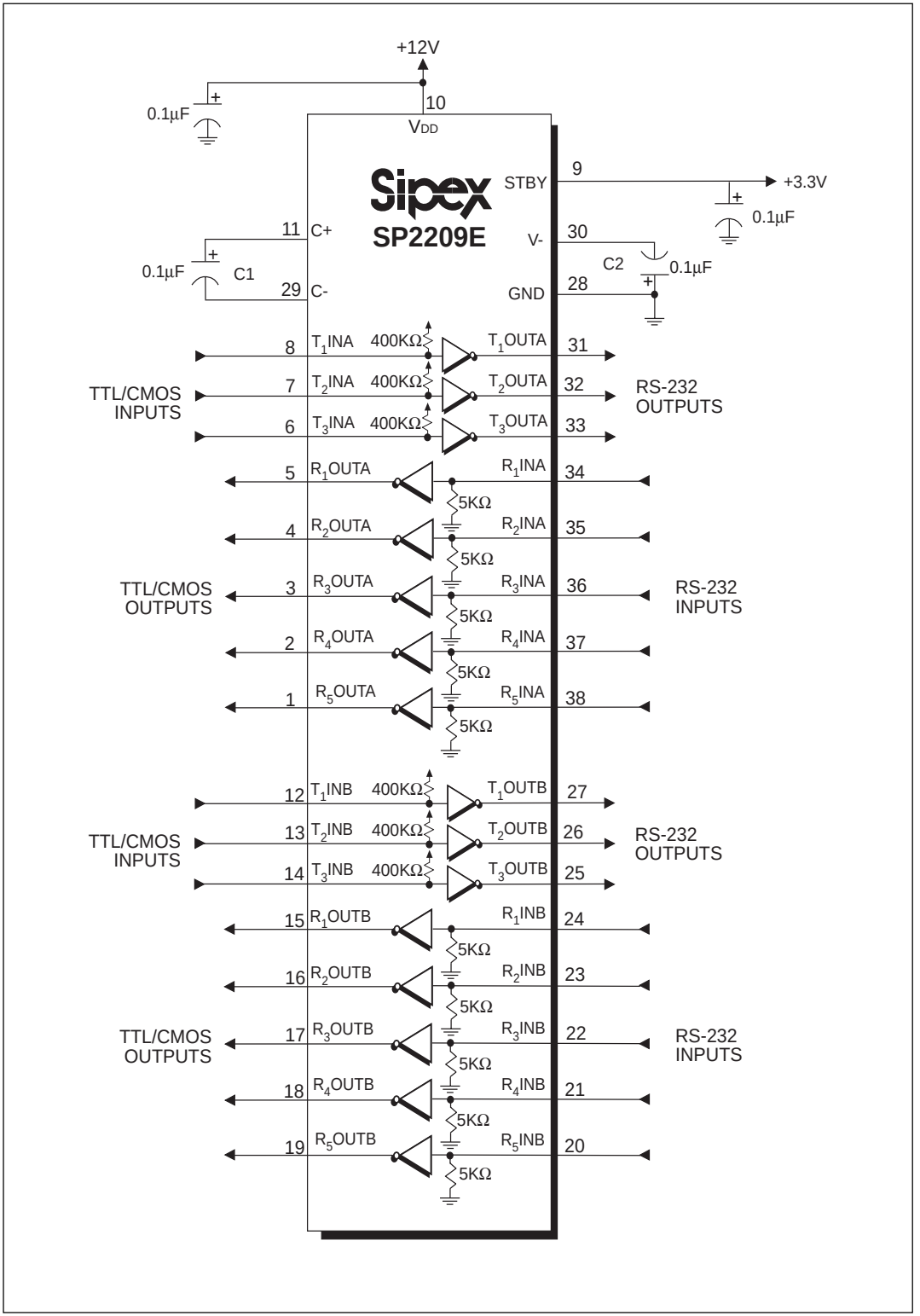


Figure 2. SP2209E Typical Operating Circuit

DESCRIPTION

The **SP2209E** device is a rugged, high ESD, complete dual RS-232 port integrated onto a single integrated circuit. Six drivers and ten receivers provide a dual port solution fully meeting the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in applications such as personal desktop computers and workstations. Refer to *Figure 2* for a typical operating circuit.

Features include high transmission rates, low power consumption, space saving package dimensions, and compatibility with the EU directive on electromagnetic compatibility. EM compatibility includes protection against radiated and conducted interference including high levels of electrostatic discharge. This device is ideal for operation in electrically harsh environments or where RS-232 cables are frequently being plugged and unplugged. This device is also immune to high RF field strengths without special shielding precautions. Emissions are also controlled to within very strict limits.

The **SP2209E** device features the inverter portion of **Sipex's** proprietary and patented (U.S. 5,306,954) on-board charge pump circuitry that generates a -9V voltage level from a single +12V power supply. The **SP2209E** device can operate at data rates of at least 460kbps fully loaded.

Its low power CMOS operation makes the **SP2209E** device an ideal choice for power sensitive designs. The **SP2209E** device has two receivers, one for each RS-232 port, that remains active in the standby mode to allow the monitoring of peripheral devices while the rest of the system is in a power-saving standby mode. This allows the **SP2209E** device to wake up the entire system when any communication is initiated in peripheral devices. The **SP2209E** device has a low standby current of 100µA.

THEORY OF OPERATION

The **SP2209E** device is made up of four basic circuit blocks: 1. Drivers, 2. Receivers, 3. the Sipex proprietary charge pump, and 4. ***Standby*** circuitry.

Drivers

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to EIA/TIA-232 levels with an inverted sense relative to the input logic levels. With V_{DD} = +12V, the typical RS-232 output voltage swing is ±9V with no load and ±5V minimum fully loaded. Unused driver input may be left unconnected with an internal pull-up resistor pulling the inputs high forcing the driver outputs into a low state. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232F and all previous RS-232 versions.

The drivers typically can operate at a minimum data rate of 460kbps fully loaded with 3KΩ in parallel with 1000pF, ensuring compatibility with PC-to-PC communication software. The **SP2209E** device is ideal for the new generation modem standards which require data rates greater than 460kbps. Refer to *Figures 3* and *5* for driver propagation delay test circuit and waveforms, respectively.

Receivers

The receivers convert EIA/TIA-232 levels to TTL or CMOS logic output levels. Should an unused receiver input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state. Receiver inputs are also protected against overvoltages of up to ±15V. Refer to *Figures 4* and *6* for receiver propagation delay test circuit and waveforms, respectively.

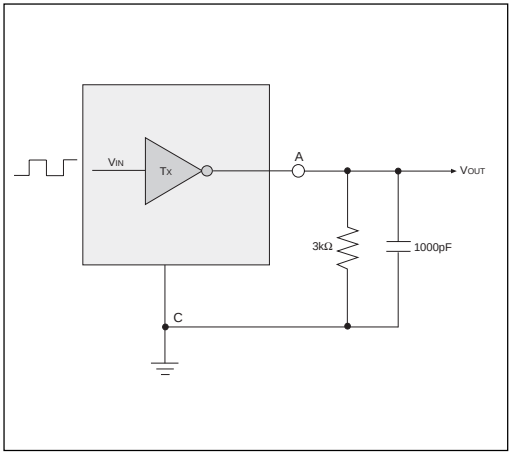


Figure 3. Driver Propagation Delay and Transition Time Test Circuit

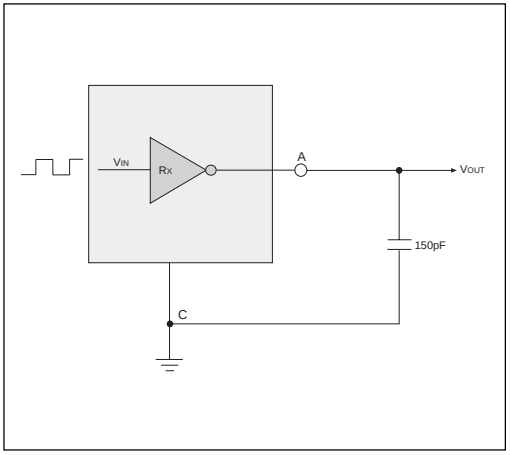


Figure 4. Receiver Propagation Delay and Transition Time Test Circuit

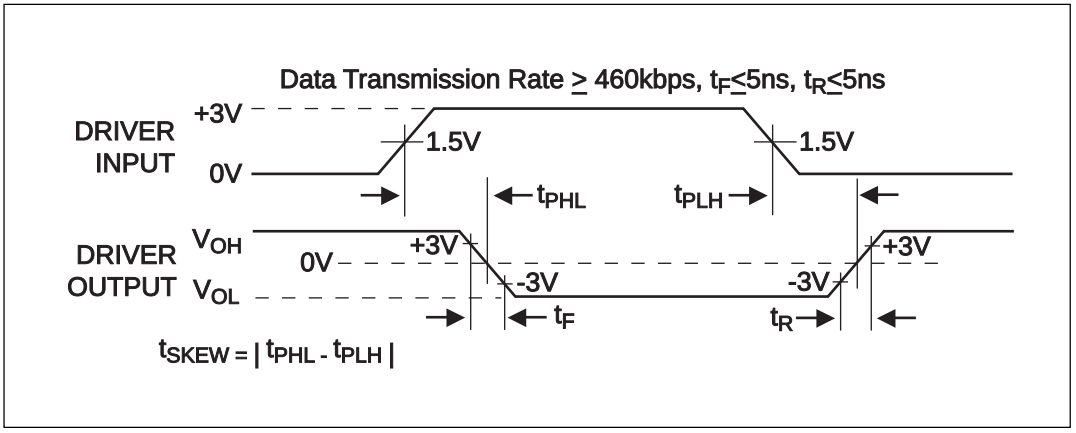


Figure 5. Driver Propagation Delays

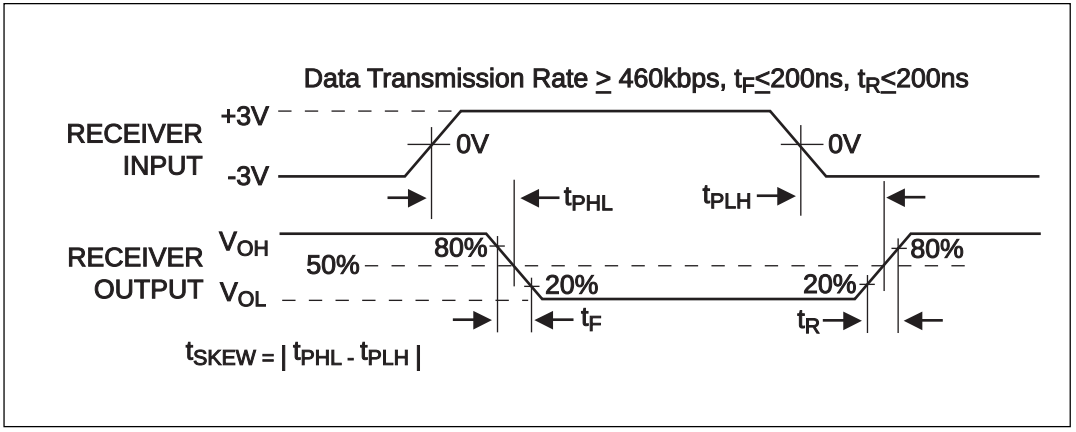


Figure 6. Receiver Propagation Delays

One receiver in each RS-232 port can be kept active by a low current, +3.3V to +5V power supply while the rest of the channels are powered down. This allows the **SP2209E** device to monitor peripheral devices while the rest of the system is in a power-saving standby mode. The **SP2209E** device can be implemented as a power management device to wake up the entire system when any communication is initiated in peripheral devices. The **SP2209E** device has a low standby current of 100µA.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines and inputs with slow transition times.

Charge Pump

The charge pump is a **Sipex**–patented design (U.S. 5,306,954) and uses a unique approach compared to older less–efficient designs. The charge pump requires two external capacitors using a two–phase voltage shifting technique with a 200kHz internal oscillator to attain a -9V power supply. Refer to *Figure 7* for the internal charge pump circuit. The internal power supply consists of a charge pump that provides output voltages of at least ±5V regardless of the input voltage (V_{DD}). This is important to maintain compliant RS-232 levels regardless of power supply fluctuations. A description of each phase follows.

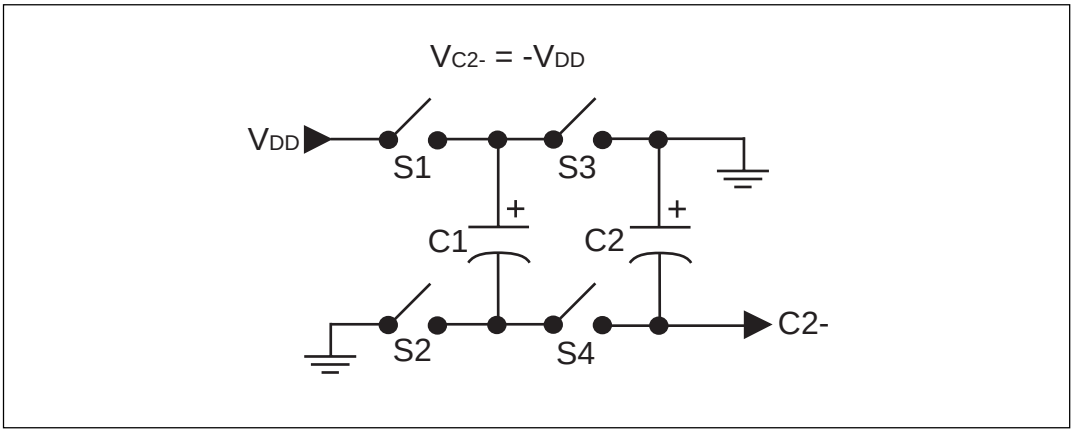


Figure 7. Charge Pump Circuit

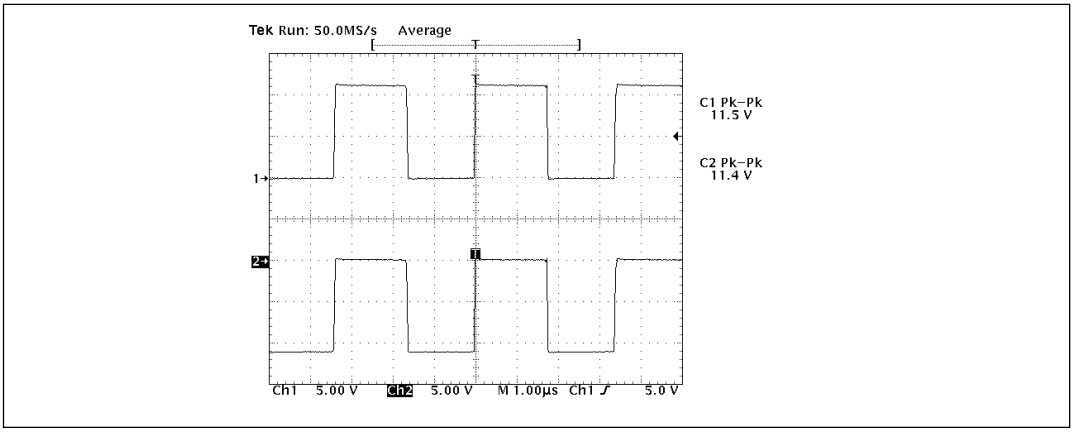


Figure 8. Charge Pump Waveforms

Phase 1

— V_{DD} charge storage — S1 and S2 are closed. S3 and S4 are open. During this phase of the clock cycle, the positive side of capacitor, C1, is connected to V_{DD}. The negative side of C1 is connected to GND. C1 is charged to $+V_{DD}$.

Phase 2

— V_{DD} transfer — S1 and S2 are open. S3 and S4 are closed. The negative side of the capacitor, C2, is connected to C2-. The positive side of C2 is connected to GND. This transfers a negative generated voltage to C2. A negative voltage is built up on the negative side of C2 with each cycle of the oscillator. If the current drawn is small, the output voltage at C2- will be close to $-V_{DD}$. As the current drawn at C2- increases, the output voltage will decrease in magnitude. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present. Refer to *Figure 8* for the internal charge pump waveforms.

Standby Circuitry

The **SP2209E** device incorporates power saving, on board standby circuitry. The standby current is typically less than 100µA. The **SP2209E** device automatically enters a standby mode when the V_{DD} power supply is removed. An internal comparator generates an internal shutdown signal that disables the internal oscillator disengaging the charge pump. Refer to *Figure 9* for the internal standby detection circuit.

The inverted output V- goes to ground. All driver outputs are disabled. The inputs of receivers 1 through 4 for both ports A and B are at high impedance. Receiver 5 for both ports A and B remain fully active as power management receiver lines to system peripherals that may come online during the standby mode.

ESD Tolerance

The **SP2209E** device incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without damage nor latch-up.

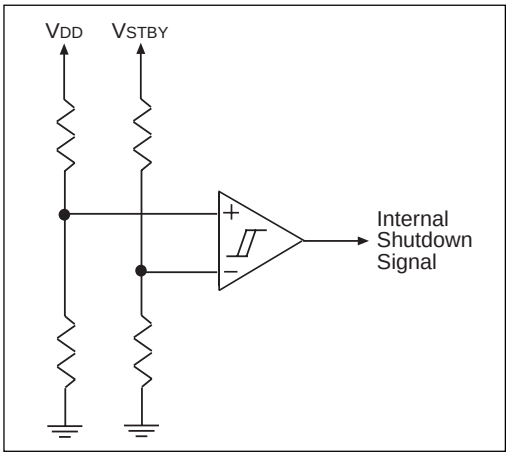


Figure 9. Internal Standby Detection Circuit

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7
b) EN61000-4-2 Air-Discharge
c) EN61000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 10*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The EN61000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with EN61000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the

equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for EN61000-4-2 is shown on *Figure 11*. There are two methods within EN61000-4-2, the Air Discharge method and the Contact Discharge method.

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit model in *Figures 10* and *11* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ an 100pF, respectively. For EN61000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω an 150pF, respectively.

The higher C_S value and lower R_S value in the EN61000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

APPLICATIONS

With six drivers and ten receivers, the **SP2209E** device is ideal for applications requiring two RS-232 ports such as in desktop or portable computers. Refer to *Figure 13*. For typical DB9 serial ports for Data Terminal Equipment (DTE)

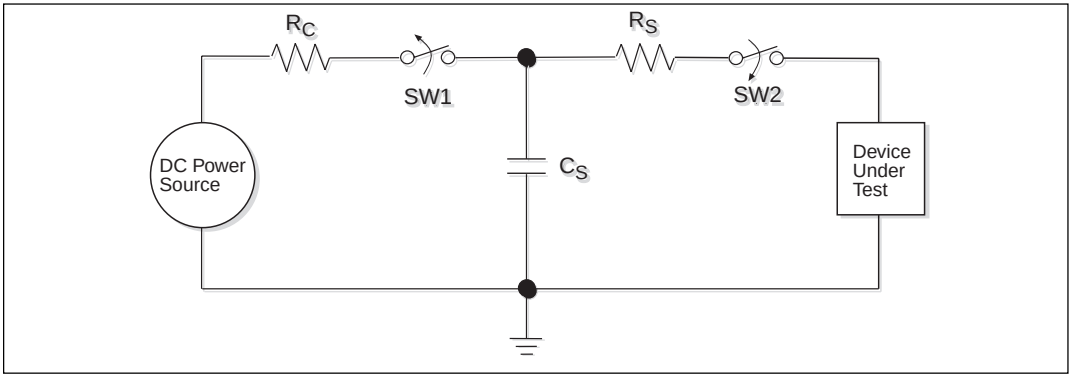


Figure 10. ESD Test Circuit for Human Body Model

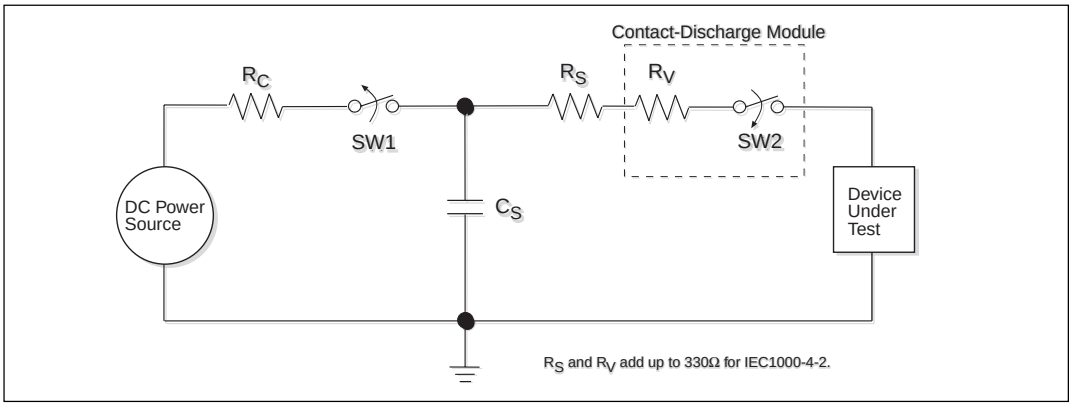


Figure 11. ESD Test Circuit for EN61000-4-2

to Data Circuit Terminating Equipment (DCE) interface implementation, 2 data lines, TxD and RxD, and 6 control lines, RTS, DTR, DSR, CTS, and RI, are required. The straight-through pinout for data lines in the **SP2209E** device allows a simplified PCB layout allowing ground lines to separate the signal lines and ground planes to be placed beneath the IC without the complication of a multi-layer PCB layout.

A receiver from each port, R_5INA and R_5INB, are active while the rest of the channels are powered down. This allows the **SP2209E** device to monitor peripheral devices while the rest of the system is in a power-saving standby mode. Fail-Safe receiver outputs are pulled high if the receiver inputs are left unconnected or at zero input. The **SP2209E** device can be implemented as a power management device to wake up the entire system when any communication is initiated in peripheral devices. The **SP2209E** device has a low standby current of 100µA.

A standard serial mouse can be powered from the **SP2209E** drivers. Two driver outputs connected in parallel and set to V_{OH} can be used to supply power to the V+ pin of the mouse. The third driver is set to VOL to link current from the V- terminal. Typical mouse specifications are 10mA at +6V and 5mA at -6V.

LapLink Compatibility

The **SP2209E** can operate up to 460kbps data rate under maximum driveload conditions of C_L = 1000pF and R_L = 3KΩ at minimum power supply voltages.

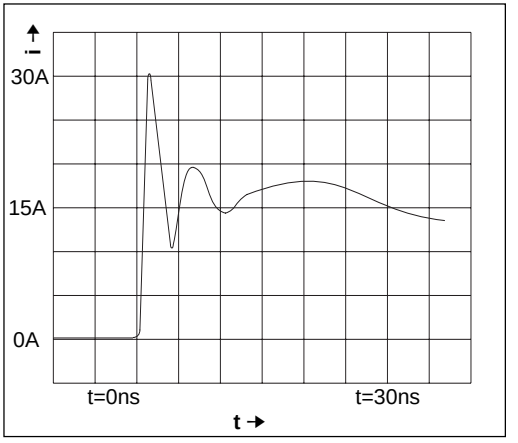


Figure 12. ESD Test Waveform for EN61000-4-2

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

Table 2. Transceiver ESD Tolerance Levels

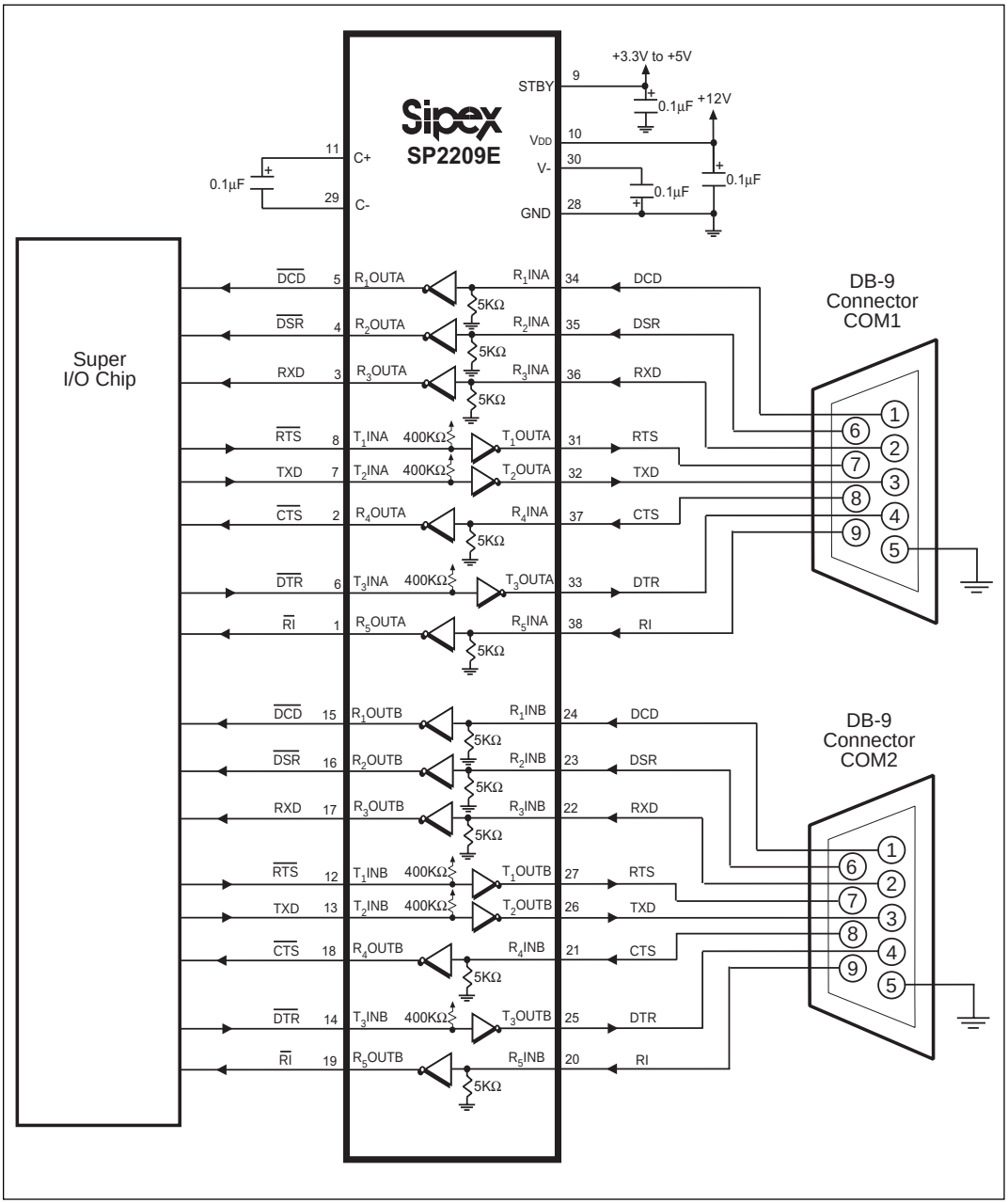
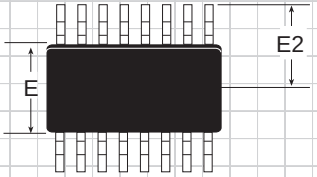
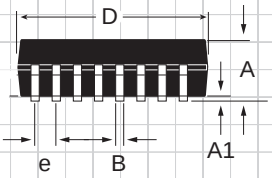
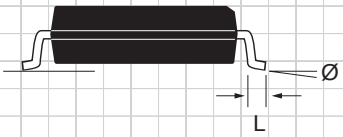


Figure 13. Dual Serial Port Application with Two DB9 Connectors

PACKAGE: PLASTIC THIN SMALL OUTLINE (TSSOP)







DIMENSIONS (mm) Minimum/Maximum	38–PIN
A	(- /1.10)
A1	(0.05/0.15)
B	(0.17/0.27)
D	(9.60/9.80)
E	(4.30/4.50)
e	(0.50 BSC)
E2	(3.20 BSC)
L	(0.50/0.75)
Ø	0°/8°

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP2209EEY	-40°C to +85°C	38-pin TSSOP

Please consult the factory for pricing and availability on a Tape-On-Reel option.

SIGNAL PROCESSING EXCELLENCE

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