M5M4V16G50DFP -8, -10, -12

16M (2-BANK x 262144-WORD x 32-BIT) Synchronous Graphics RAM

PRELIMINARY

Some of contents are described for general products and are subject to change without notice.

DESCRIPTION

The M5M4V16G50DFP is a 2-bank x 262,144-word x 32-bit Synchronous GRAM, with LVTTL interface. All inputs and outputs are referenced to the rising edge of CLK. The M5M4V16G50DFP can operate at frequencies of 100+ MHz. The BLOCK WRITE and WRITE-PER-BIT functions provide improved performance in graphic memory systems.

FEATURES

- Single 3.3v±0.3v power supply
- Clock frequencies of 125 MHz
- Fully synchronous operation referenced to clock rising edge
- Dual bank operation controlled by A10(Bank Address)
- Internal pipelined operation: column address can be changed every clock cycle
- Programmable /CAS Latency (**LVTTL:** 2 and 3)
- Programmable Burst Length (1/2/4/8 and Full Page)
- Programmable Burst Type (Sequential / Interleave)
- Byte control using DQM0 - DQM3 signals in both read and write cycles
- Persistent Write-Per-Bit (WPB) function
- 8 Column Block Write (BW) function
- Auto Precharge / All bank precharge controlled by A9
- Auto Refresh and Self Refresh Capability
- 2048 refresh cycles /32ms
- LVTTL Interface
- 100 pin QFP package with 0.65mm lead pitch

	Max. Frequency	CLK Access Time
M5M4V16G50DFP - 8	125MHz	7ns
M5M4V16G50DFP- 10	100MHz	8ns
M5M4V16G50DFP- 12	83MHz	10ns

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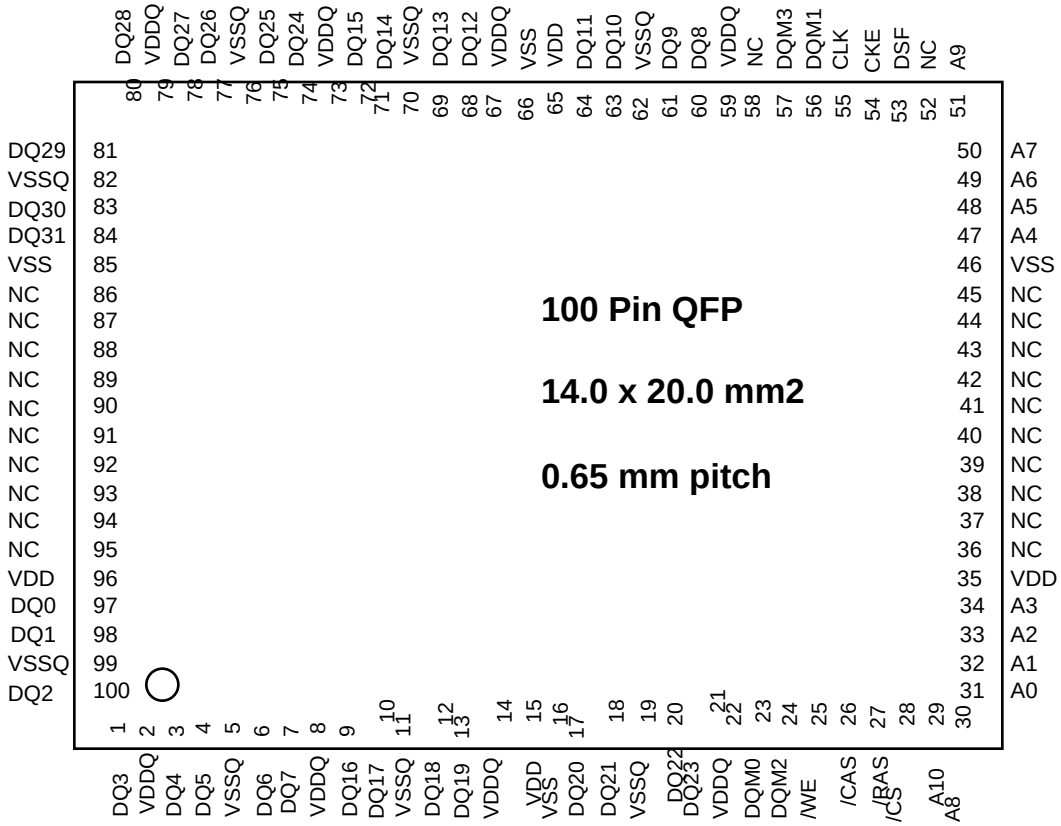

CLK	**: Master Clock**
CKE	**: Clock Enable**
/CS	**: Chip Select**
/RAS	**: Row Address Strobe**
/CAS	**: Column Address Strobe**
/WE	**: Write Enable**
DSF	**: Special Function Enable**
A0-10	**: Address Input**
A0-9	**: Row Address inputs**
A0-7	**: Column Address inputs**
A10	**: Bank Address**
DQ0-31	**: Data I/O**
DQM0-3	**: Output Disable/ Write Mask**
Vdd	**: Power Supply**
VddQ	**: Power Supply for Output**
Vss	**: Ground**
VssQ	**: Ground for Output**

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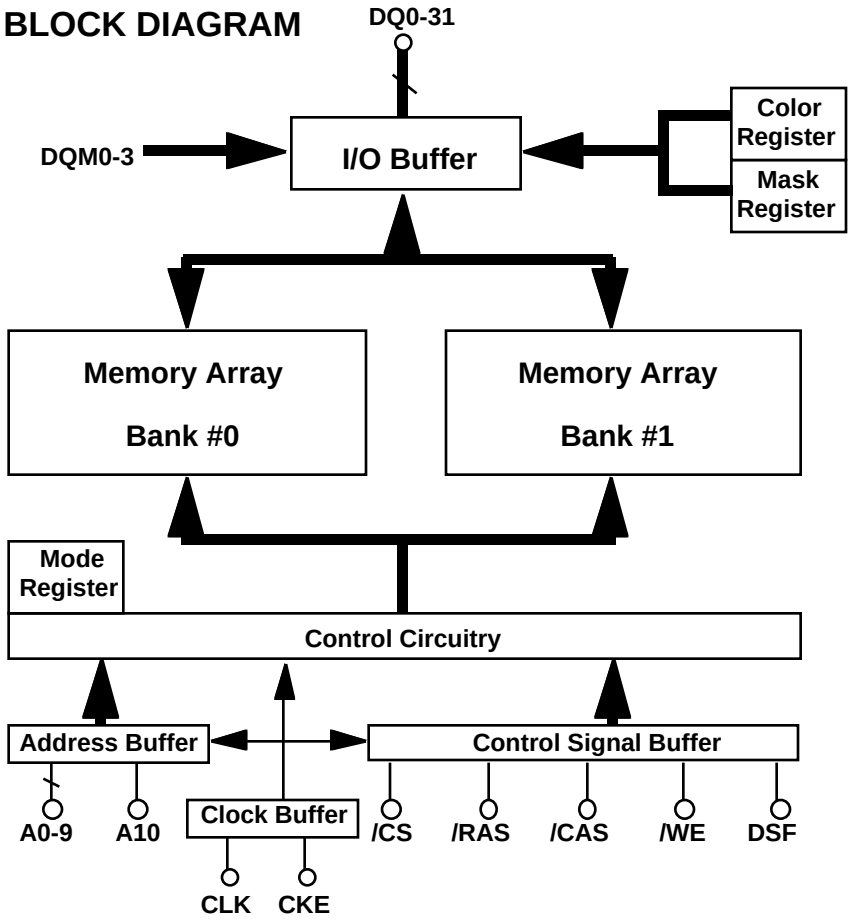
BLOCK DIAGRAM



Type Designation Code

This rule is applied only to Synchronous DRAM family.

M 5M 4 V 16 G 5 0 D FP - 8

- Cycle Time (min.) 8: 8ns, 10: 10ns, 12: 12ns
- Package Type FP: QFP
- Process Generation
- Function 0: Random Column, 1: 2N-rule
- Organization 2^n 5: x32
- **Synchronous Graphics RAM**
- Density 16:16M bits
- Interface V:LVTTL
- Memory Style (DRAM)
- Use, Recommended Operating Conditions, etc
- Mitsubishi Main Designation

PIN FUNCTION

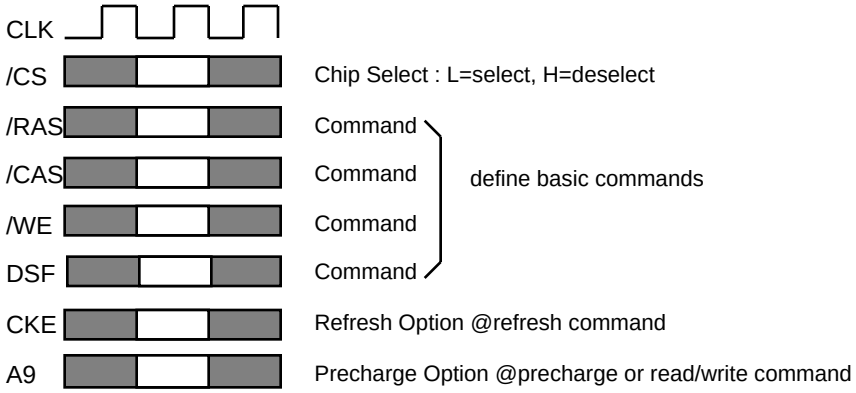
CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK.
CKE	Input	Clock Enable: CKE controls internal clock. When CKE is low, internal clock for the following cycle is stopped. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE becomes asynchronous input. Self refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, / WE, and DSF	Input	Combination of /RAS, /CAS, /WE, and DSF defines basic commands.
A0-9	Input	A0-9 specify the Row / Column Address in conjunction with BA. The Row Address is specified by A0-9. The Column Address is specified by A0-7. A9 is also used to indicate precharge option. When A9 is high at a read / write command, an auto precharge is performed. When A9 is high at a precharge command, both banks are precharged.
A10	Input	Bank Address: A10 (BA) specifies the bank to which a command is applied. A10 (BA) must be set with ACT, PRE, READ, WRITE commands.
DQ0-31	Input / Output	Data In/Data out are referenced to the rising edge of CLK. These pins are used for input mask pins for Write-Per-Bit and column/byte mask inputs for Block Writes.
DQM0 - DQM3	Input	Input/Output Byte Mask: When DQM0-3 are high during a write, data for the current cycle is masked. When DQM0-3 are high during a read, output data is disabled at the next cycle. DQM0 controls byte 0 (DQ7-0), DQM1 controls byte 1 (DQ15-8), DQM2 controls byte 2 (DQ23-16), and DQM3 controls byte 3 (DQ31-24).
VREF	Input	Reference voltage for all inputs.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.

BASIC FUNCTIONS

The M5M4V16G50DFP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS, /CAS, /WE, and DSF at CLK rising edge. In addition to 3 signals, /CS ,CKE and A9 are used as chip select, refresh option, and precharge option, respectively.

For a more detailed definition of commands, please see the command truth table.



Activate (ACT) [/CS, /RAS, DSF = L, /CAS, /WE = H]

ACT command activates a row in an idle bank indicated by A10 (BA) and row address selected by A0 - A9.

Activate with WPB enable (ACTWPB) [/CS, /RAS = L, /CAS, /WE, DSF = H]

This command is the same as Activate except that Write-Per-Bit (WPB) is enabled. The Mask Register's contents are used as the WPB data.

Read (READ) [/CS, /CAS, DSF = L, /RAS, /WE = H]

READ command starts burst read from the active bank indicated by A10 (BA). First output data appears after /CAS latency. When A9 = H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**).

Write (WRITE) [/CS, /CAS, /WE, DSF = L, /RAS = H]

WRITE command starts burst write to the active bank indicated by A10 (BA). Total data length to be written is set by burst length. When A9 = H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

Precharge (PRE) [/CS, /RAS, /WE, DSF = L, /CAS = H]

PRE command deactivates the active bank indicated by A10 (BA). This command also terminates burst read /write operation. When A9 = H at this command, both banks are deactivated (precharge all, **PREA**).

BASIC FUNCTIONS (continued)

Auto-Refresh (REFA) [/CS, /RAS, /CAS, DSF = L, /WE, CKE = H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically. Both banks must be precharged before this command can begin.

Self-Refresh (REFS) [/CS, /RAS, /CAS, DSF, CKE = L, /WE = H]

REFS command starts self-refresh cycle. The self-refresh cycle will continue while CKE remains low. When CKE goes high, self-refresh is exited. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically. Both banks must be precharged before this command can begin.

Burst Terminate (TERM) [/CS, /WE, DSF = L, /RAS, /CAS = H]

TERM command stops the current burst operation. During read cycles, burst data stops after CAS latency is met.

No Operation (NOP) [/CS, DSF = L, /RAS, /CAS, /WE = H]

NOP command does not perform any operation on the SGRAM.

Mode Register Set (MRS) [/CS, /WE, /RAS, /CAS, DSF = L]

MRS command loads the mode register that defines how the device operates. The address pins, A0 - A10, are used as input pins for the mode register data. This command must be issued after power-on to initialize the SGRAM. The mode register can only be set when both banks are idle. During the two cycles following this command, the SGRAM cannot accept any other commands.

Special Register Set (SRS) [/CS, /WE, /RAS, /CAS = L, DSF = H]

SRS command sets the color and mask registers. During the two cycles following this command, the SGRAM cannot accept any other commands.

Masked Block Write (BW) [/CS, /CAS, /WE = L, /RAS, DSF = H]

BW command starts the 8 column Block Write function. Burst Length = 1 is assumed. Write data comes from the color register and column address mask data is applied on the DQs. When A9 = H at this command, the bank is deactivated after the burst write (auto-precharge, **BWA**).

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DSF	A10	A9	A0-8
Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	L	X	X	X
Row Address Entry & Bank Activate	ACT	H	X	L	L	H	H	L	BA	Row	Add.
Row Address Entry & Bank Activate	ACTWPB	H	X	L	L	H	H	H	BA	Row	Add.
Single Bank Precharge	PRE	H	X	L	L	H	L	L	BA	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	L	X	H	X
Column Address Entry & Write	WRITE	H	X	L	H	L	L	L	BA	L	Col.
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	L	BA	H	Col.
Column Address Entry & Masked Block Write	BW	H	X	L	H	L	L	H	BA	L	Col.
Masked Block Write with Auto-Precharge	BWA	H	X	L	H	L	L	H	BA	H	Col.
Column Address Entry & Read	READ	H	X	L	H	L	H	L	BA	L	Col.
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	L	BA	H	Col.
Auto-Refresh	REFA	H	H	L	L	L	H	L	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	L	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	X
		L	H	L	H	H	H	L	X	X	X
Burst Terminate	TERM	H	X	L	H	H	L	L	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	OPCODE		
Special Register Set	SRS	H	X	L	L	L	L	H	OPCODE		

H=High Level, L=Low Level, BA=Bank Address, Col.=Column Address (A0-A7)
Row Add.=Row Address (A0-A9), X=Don't Care, n=CLK cycle number

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action
IDLE	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	L	X	NOP	NOP
	L	H	H	L	H	X	Undefined	ILLEGAL
	L	H	H	L	L	X	TERM	ILLEGAL*2
	L	H	L	H	H	X	Undefined	ILLEGAL
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL*2
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL*2
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL*2
	L	L	H	H	L	BA, RA	ACT	Bank Active; Latch RA; No Mask
	L	L	H	H	H	BA, RA	ACTWPB	Bank Active; Latch RA; Use Mask
	L	L	H	L	H	X	Undefined	ILLEGAL
	L	L	H	L	L	BA, A9	PRE / PREA	NOP*4
	L	L	L	H	H	X	Undefined	ILLEGAL
	L	L	L	H	L	X	REFA	Auto-Refresh*5
	L	L	L	L	H	Op-Code, Mode-Add	SRS	Special Register Set*5
	L	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	L	X	NOP	NOP
	L	H	H	L	L	BA	TERM	NOP
	L	H	L	H	L	BA, CA, A9	READ / READA	Begin Read; Latch CA; Determine Auto-Precharge
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	Begin Write; Latch CA; Determine Auto-Precharge
	L	H	L	L	H	BA, CA, A9	BW / BWA	Block Write; Latch CA; Determine Auto-Precharge
	L	L	H	H	L	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	H	H	BA, RA	ACTWPB	Bank Active / ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	Precharge / Precharge All
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	Special RegisteSet *5
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action
READ	H	X	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	L	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	L	BA	TERM	Terminate Burst
	L	H	L	H	L	BA, CA, A9	READ / READA	Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge*3
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	H	L	L	H	BA, CA, A9	BW / BWA	Terminate Burst, Latch CA, Block Write, Determine Auto-Precharge*3
	L	L	H	H	L	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	H	L	BA, RA	ACTWPB	Bank Active / ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	H	X	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	L	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	L	BA	TERM	Terminate Burst
	L	H	L	H	L	BA, CA, A9	READ / READA	Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge*3
	L	H	L	L	L	BA, CA, A89	WRITE / WRITEA	Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3
	L	H	L	L	L	BA, CA, A9	BW / BWA	Terminate Burst, Latch CA, Block Write, Determine Auto-Precharge*3
	L	L	H	H	L	BA, RA	ACTWPB	Bank Active / ILLEGAL*2
	L	L	H	H	L	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action
READ with AUTO PRECHARGE	H	X	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	L	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	L	BA	TERM	ILLEGAL
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL
	L	L	H	H	L	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	H	H	BA, RA	ACTWPB	Bank Active / ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	ILLEGAL*2
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	L	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	L	BA	TERM	ILLEGAL
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL
	L	L	H	H	L	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	H	H	BA, RA	ACTWPB	Bank Active / ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	ILLEGAL*2
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	X	DESEL	NOP (Idle after tRP)
	L	H	H	H	L	X	NOP	NOP (Idle after tRP)
	L	H	H	L	L	BA	TERM	ILLEGAL*2
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL*2
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL*2
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL*2
	L	L	H	H	L	BA, RA	ACT	ILLEGAL*2
	L	L	H	H	L	BA, RA	ACTWPB	ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	NOP*4 (Idle after tRP)
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	X	DESEL	NOP (Row Active after tRCD)
	L	H	H	H	L	X	NOP	NOP (Row Active after tRCD)
	L	H	H	L	L	BA	TERM	ILLEGAL*2
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL*2
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL*2
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL*2
	L	L	H	H	L	BA, RA	ACT	ILLEGAL*2
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	ILLEGAL*2
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action
WRITE RE-COVERING	H	X	X	X	X	X	DESEL	NOP
	L	H	H	H	L	X	NOP	NOP
	L	H	H	L	L	BA	TERM	ILLEGAL*2
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL*2
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL*2
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL*2
	L	L	H	H	L	BA, RA	ACT	ILLEGAL*2
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL*2
	L	L	H	L	L	BA, A9	PRE / PREA	ILLEGAL*2
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
RE-FRESHING	H	X	X	X	X	X	DESEL	NOP (Idle after tRC)
	L	H	H	H	L	X	NOP	NOP (Idle after tRC)
	L	H	H	L	L	BA	TERM	ILLEGAL
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL
	L	L	H	H	L	BA, RA	ACT	ILLEGAL
	L	L	H	H	L	BA, RA	ACT	ILLEGAL
	L	L	H	L	L	BA, A9	PRE / PREA	ILLEGAL
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	DSF	Address	Command	Action
MODE REGISTER SETTING	H	X	X	X	X	X	DESEL	NOP (Idle after tRSC)
	L	H	H	H	L	X	NOP	NOP (Idle after tRSC)
	L	H	H	L	L	BA	TERM	ILLEGAL
	L	H	L	H	L	BA, CA, A9	READ / READA	ILLEGAL
	L	H	L	L	L	BA, CA, A9	WRITE / WRITEA	ILLEGAL
	L	H	L	L	H	BA, CA, A9	BW / BWA	ILLEGAL
	L	L	H	H	L	BA, RA	ACT	ILLEGAL
	L	L	H	H	H	BA, RA	ACTWPB	ILLEGAL
	L	L	H	L	L	BA, A9	PRE / PREA	ILLEGAL
	L	L	L	H	L	X	REFA	ILLEGAL
	L	L	L	L	H	Op-Code, Mode-Add	SRS	ILLEGAL
	L	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care
BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	DSF	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	X	ILLEGAL
	L	H	L	H	L	X	X	X	ILLEGAL
	L	H	L	L	X	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	X	NOP (Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	L	X	Enter Self-Refresh
	H	L	H	X	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	X	Enter Power Down
	H	L	L	H	H	L	X	X	ILLEGAL
	H	L	L	H	L	X	X	X	ILLEGAL
	H	L	L	L	X	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	X	Begin CLK Suspend at Next Cycle*3
	L	H	X	X	X	X	X	X	Exit CLK Suspend at Next Cycle*3
	L	L	X	X	X	X	X	X	Maintain CLK Suspend

ABBREVIATIONS:
H=High Level, L=Low Level, X=Don't Care

NOTES:
1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously** . A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

POWER ON SEQUENCE

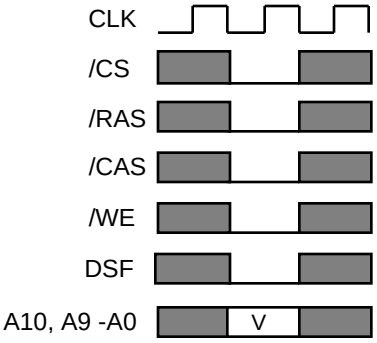
Before starting normal operation, the following power on sequence is necessary to prevent a SGRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM0-3 high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 500µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SGRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when both banks are in idle state. After tRSC from a MRS command, the SGRAM is ready for new command.



A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	LTMODE				BT	BL	

CL	CAS LATENCY
	LVTTL
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

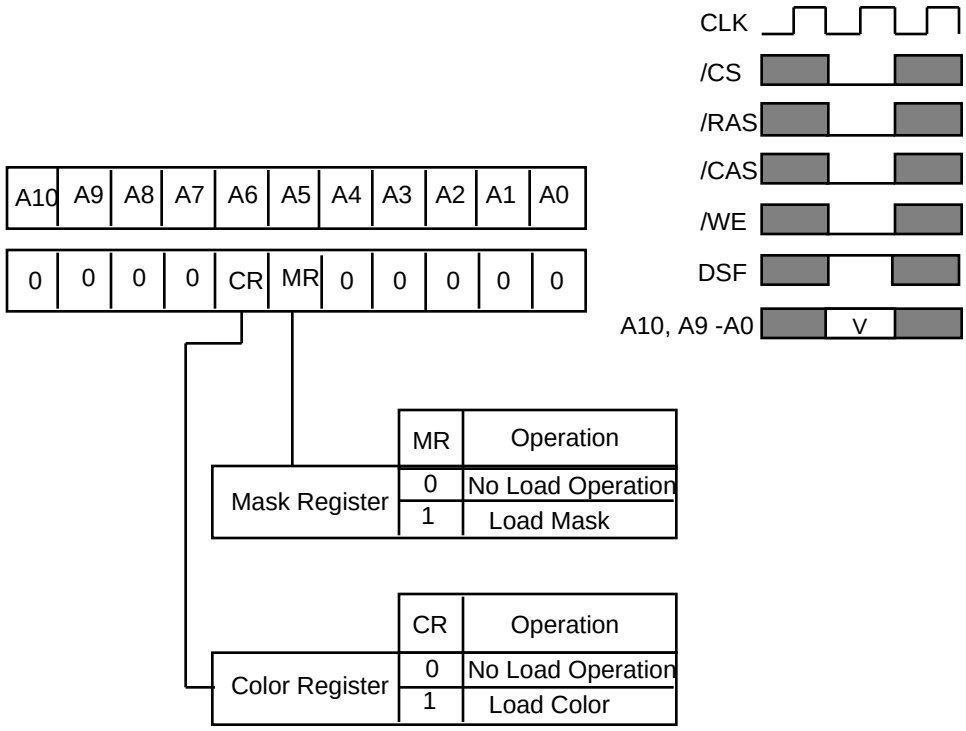
BL	BURST LENGTH	
	BT= 0	BT= 1
0 0 0	1	Reserved
0 0 1	2	Reserved
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

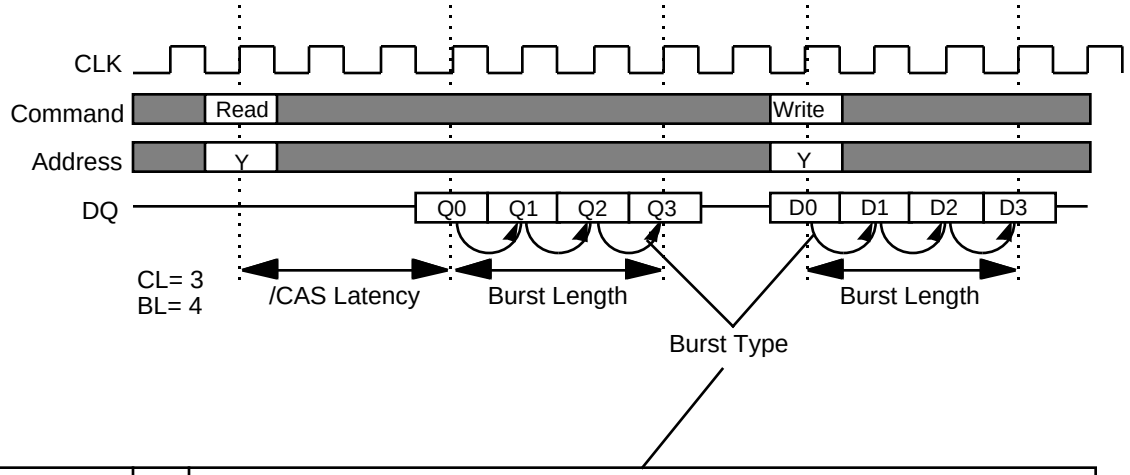
A10	A9	A8	A7	Operating Mode
0	0	0	0	Normal Operation
0	1	0	0	Burst Read and Single Write
-	-	-	-	All Others are Reserved

BURST TYPE		
	0	SEQUENTIAL
	1	INTERLEAVED

SPECIAL REGISTER

The Mask Register and Color Register can be loaded by setting the special register (SRS). If CR and MR are both high, data in the Mask and Color Registers will be unknown.After tRSC from a SRS command, the SGRAM is ready for new command.





Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

NOTE:
FULL PAGE BURST is an extension of the above tables of Sequential Addressing with the length being 256.

OPERATIONAL DESCRIPTION

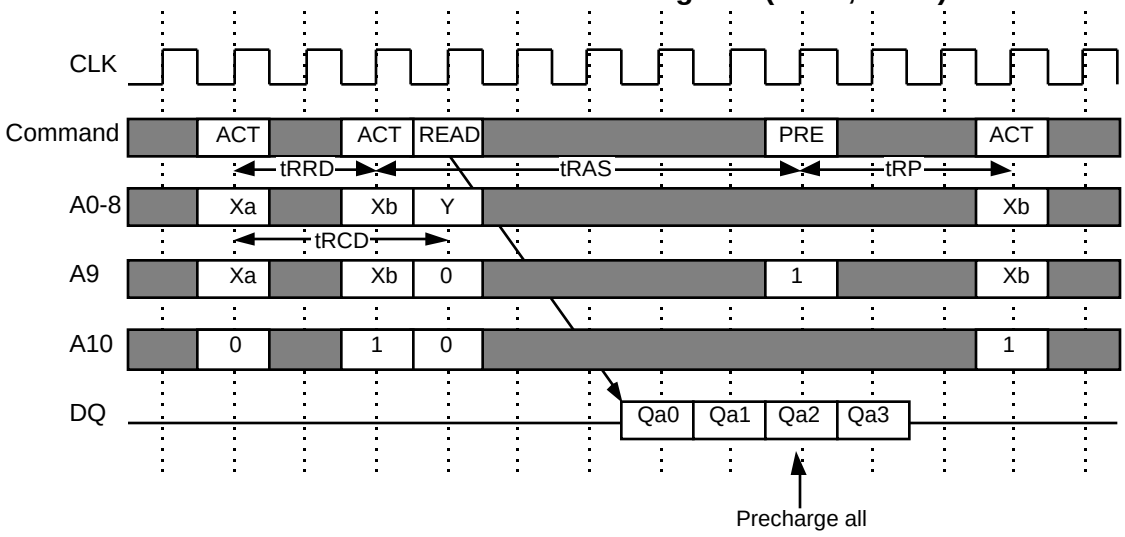
BANK ACTIVATE

The SGRAM has two independent banks. Each bank is activated by the ACT command with the bank address (A10/BA). A row is indicated by the row address A9-0. The minimum activation interval between one bank and the other bank is tRRD.

PRECHARGE

The PRE command deactivates the bank indicated by A10/BA. When both banks are active, the precharge all command (PREA, PRE + A9=H) is available to deactivate them at the same time. After tRP from the precharge, an ACT command can be issued.

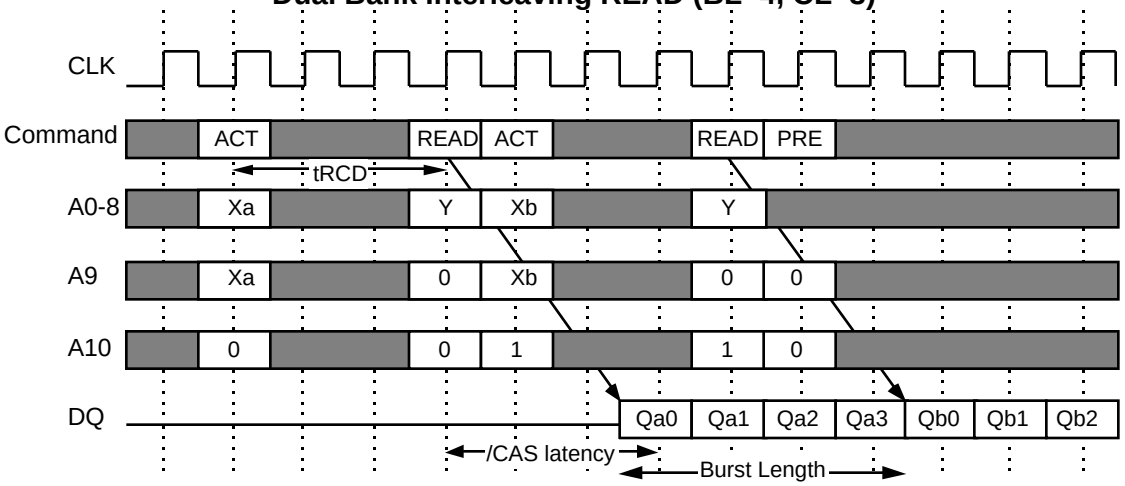
Bank Activation and Precharge All (BL=4, CL=3)



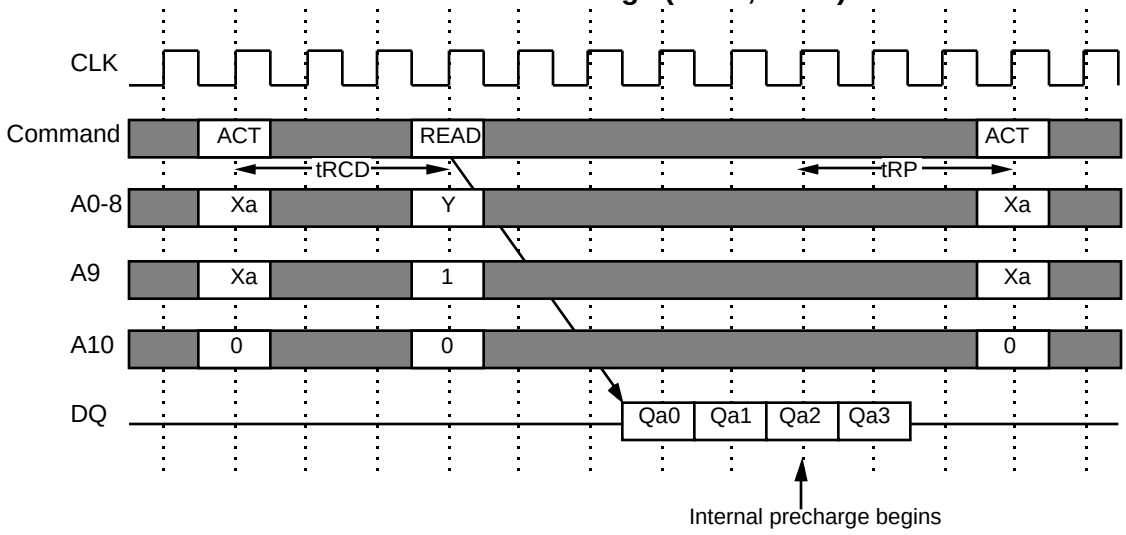
READ

After tRCD from the bank activation, a READ command can be issued. 1st output data is available after the /CAS Latency from the READ, followed by (BL -1) consecutive data when the Burst Length is BL. The start address is specified by A7-0, and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data (in case of BL=4) by interleaving the dual banks. When A9 is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited until the internal precharge is complete. The internal precharge start timing depends on /CAS Latency. The next ACT command can be issued after tRP from the internal precharge timing.

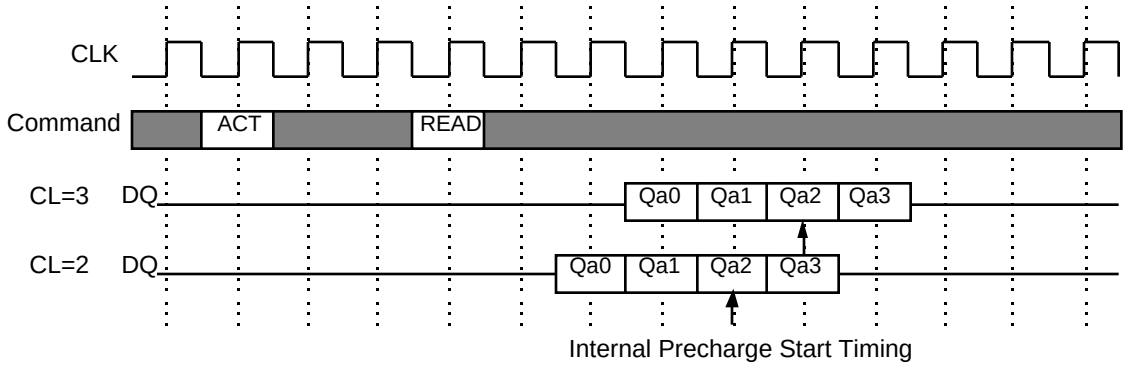
Dual Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



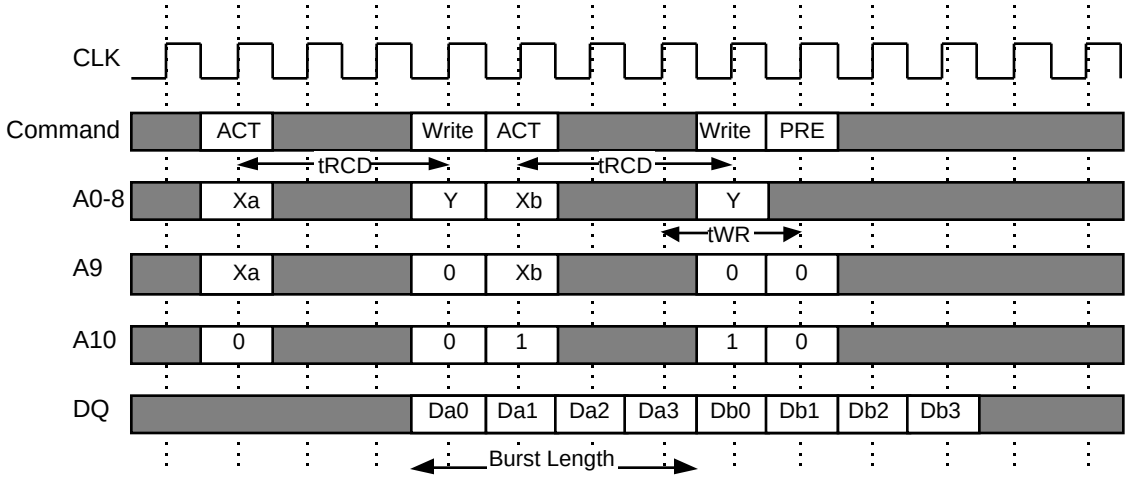
READ Auto-Precharge Timing (BL=4)



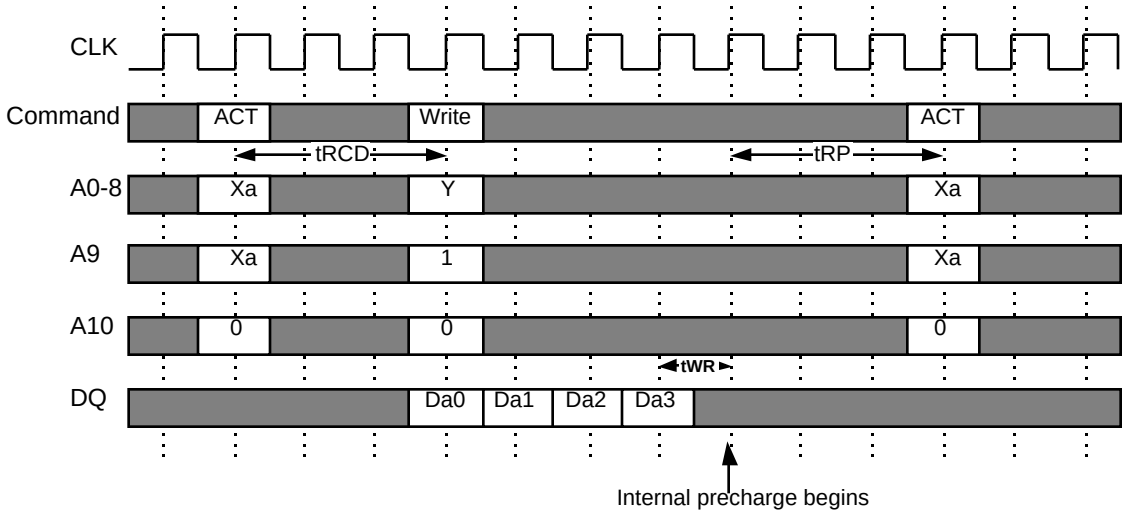
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set in the same cycle as the WRITE. The following (BL -1) data is written into the RAM, when the Burst Length is BL. The start address is specified by A7-0, and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data (in case of BL=4) by interleaving the dual banks. When A9 is high at a WRITE command, the auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT) to the same bank is inhibited until the internal precharge is complete. The internal precharge begins at tWR after the last input datacycle. The next ACT command can be issued after tRP from the internal precharge timing.

Dual Bank Interleaving WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

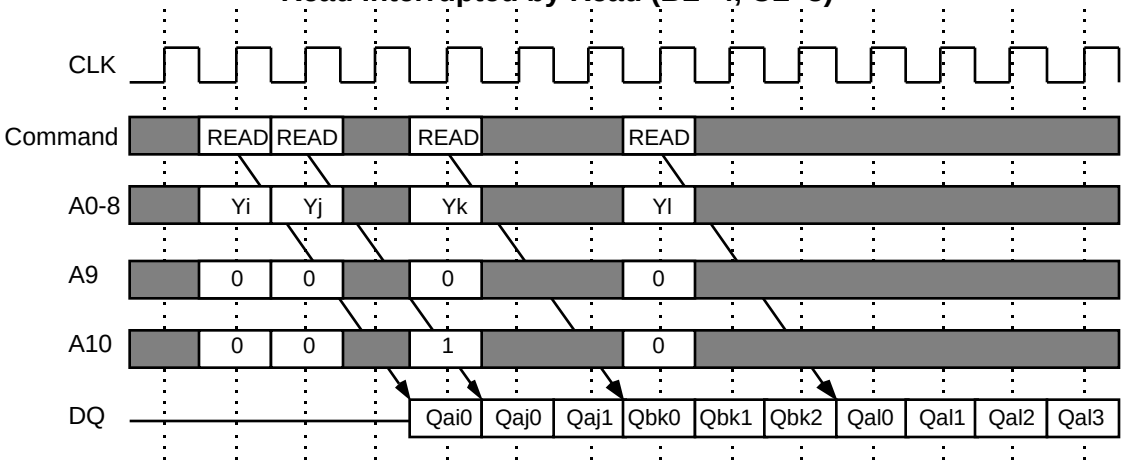


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read operation can be interrupted by new read of the same or the other bank. M5M4V16G50DFP allows random column access. READ to READ interval is minimum 1 CLK.

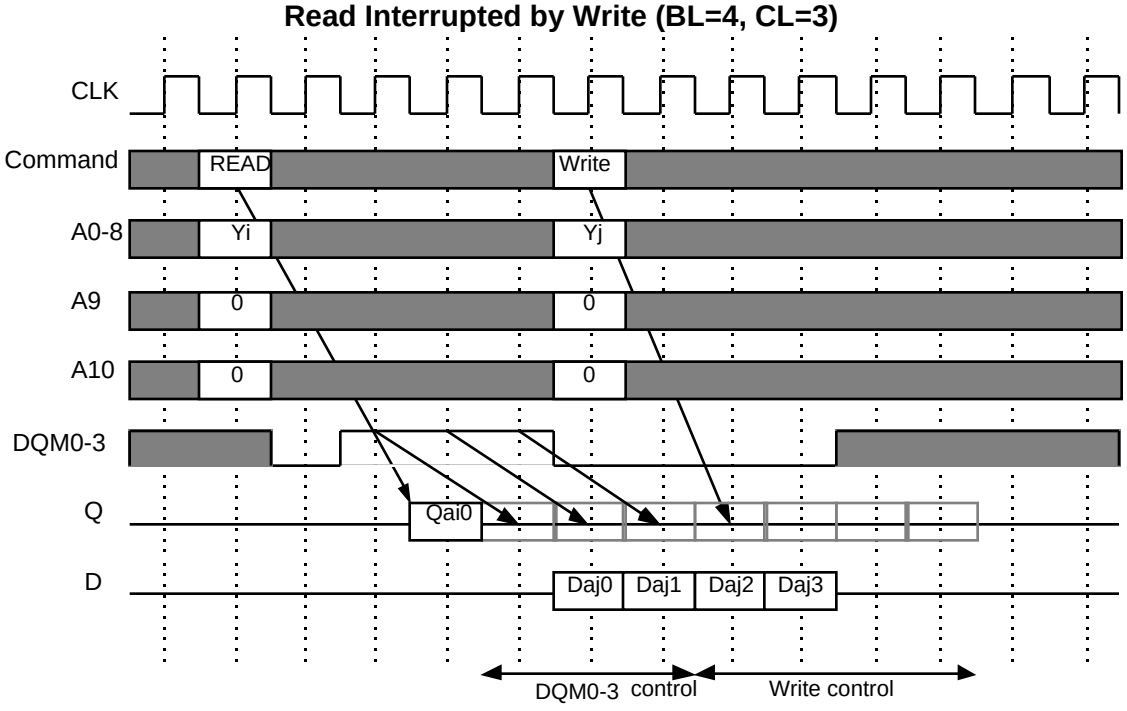
Read Interrupted by Read (BL=4, CL=3)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of the same or the other bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM0 - 3 to prevent bus contention. The output is disabled automatically 2 cycles after WRITE assertion.

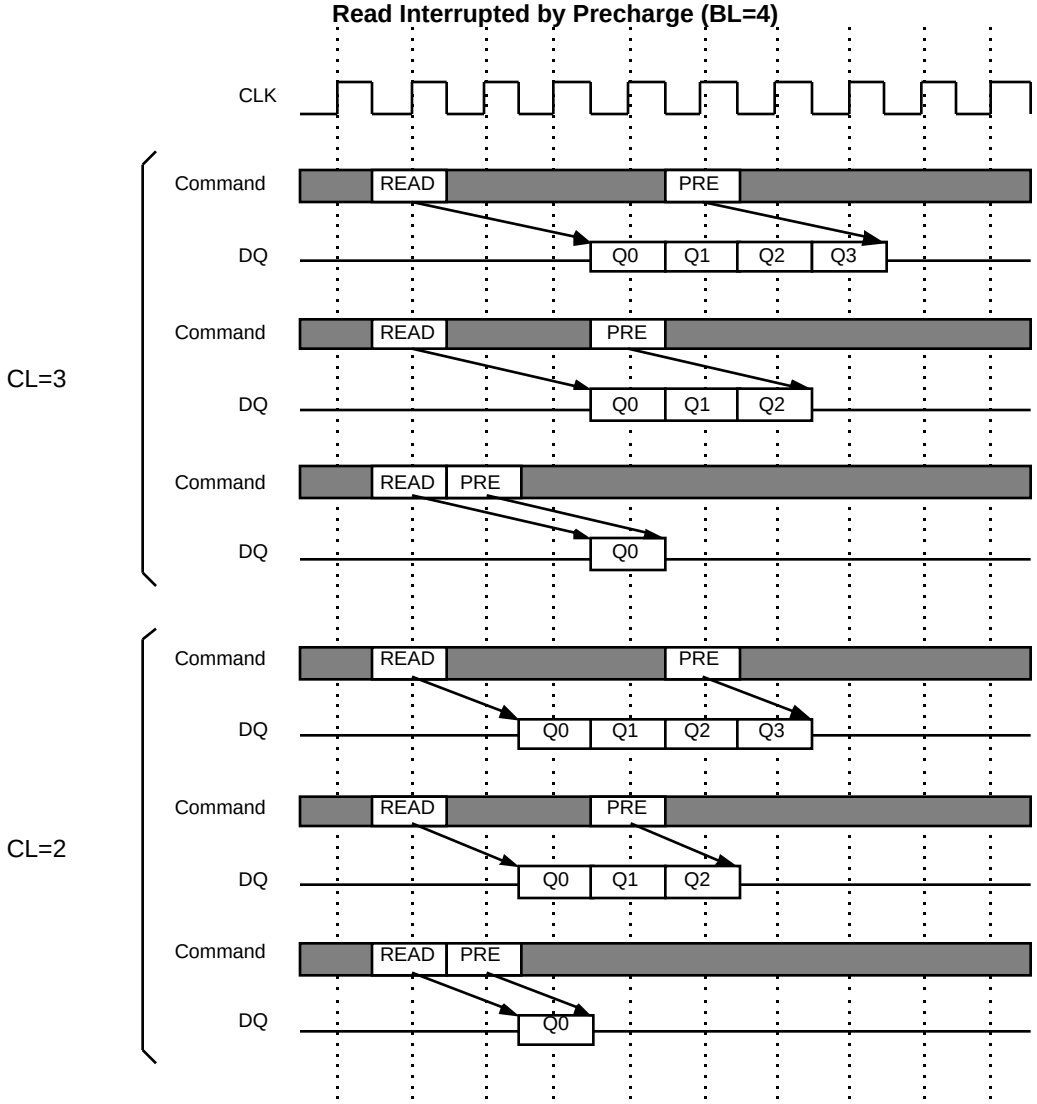
Read Interrupted by Write (BL=4, CL=3)



[Read Interrupted by Precharge]

Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command disables the data output depending on the /CAS Latency. The figure below shows examples of when the dataout is terminated.

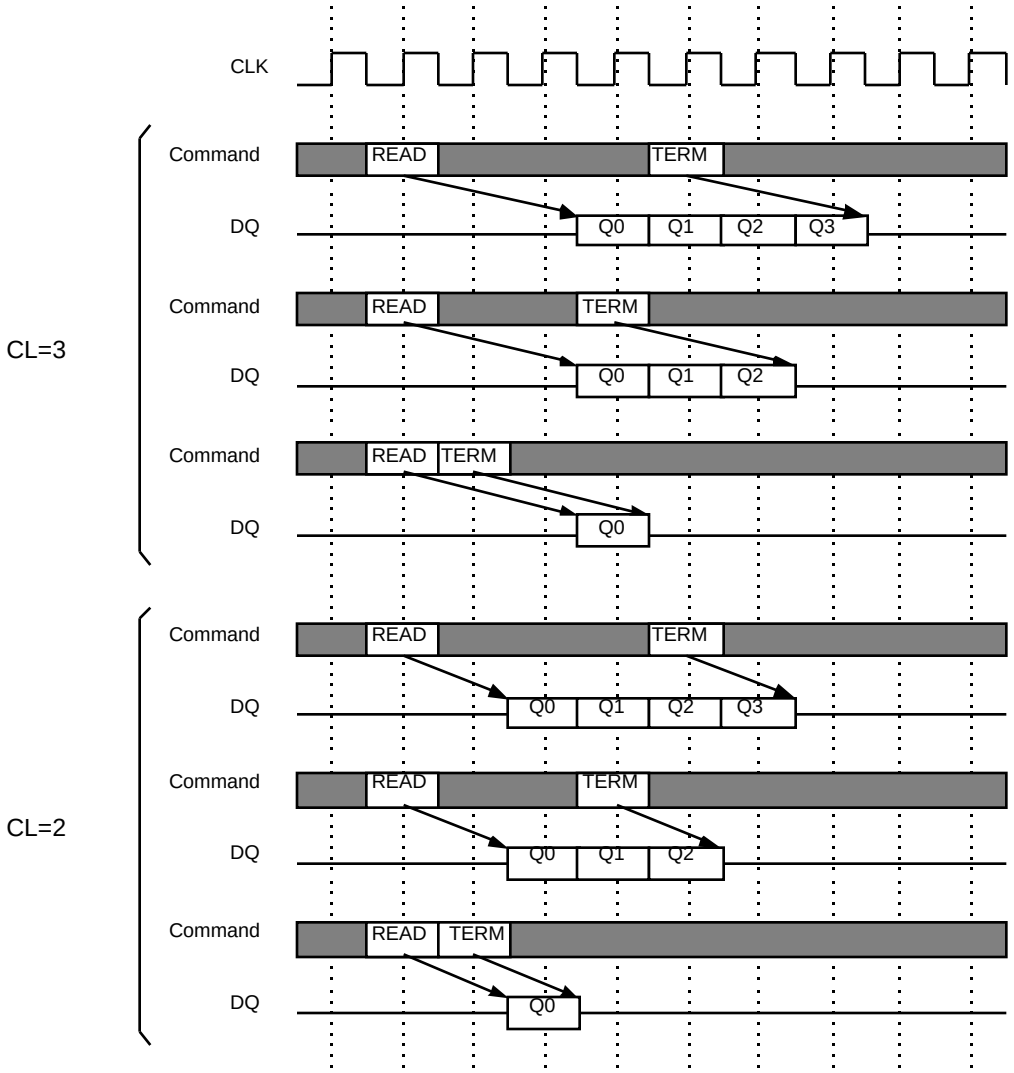
Read Interrupted by Precharge (BL=4)



[Read Interrupted by Burst Terminate]

Similarly to the precharge, burst terminate command can interrupt burst read operation and disable the data output. READ to TERM interval is minimum 1 CLK. The figure below shows examples when the dataout is terminated.

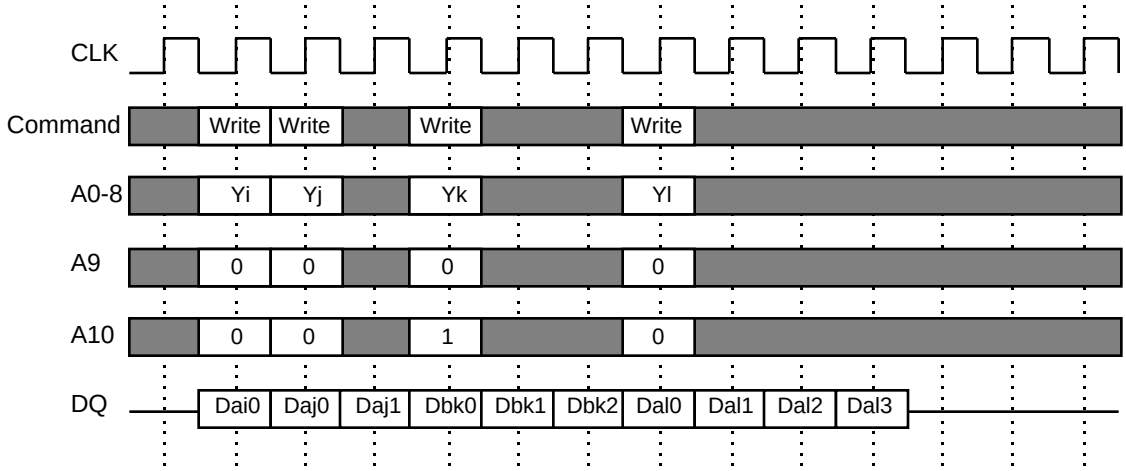
Read Interrupted by Burst Terminate (BL=4)



[Write Interrupted by Write]

Burst write operation can be interrupted by new write of the same or the other bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

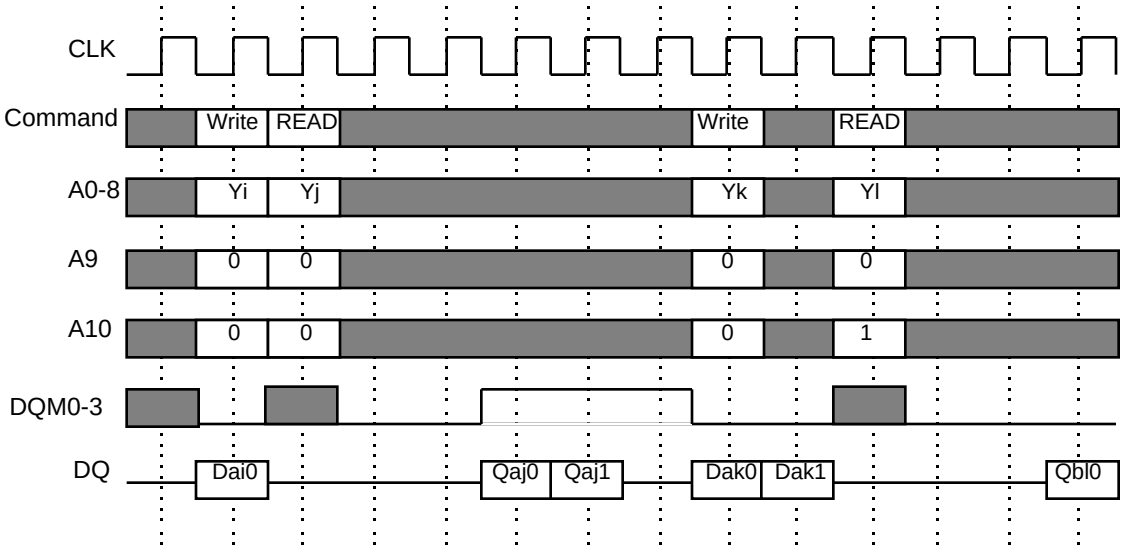
Write Interrupted by Write (BL=4)



[Write Interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is “don’t care”.

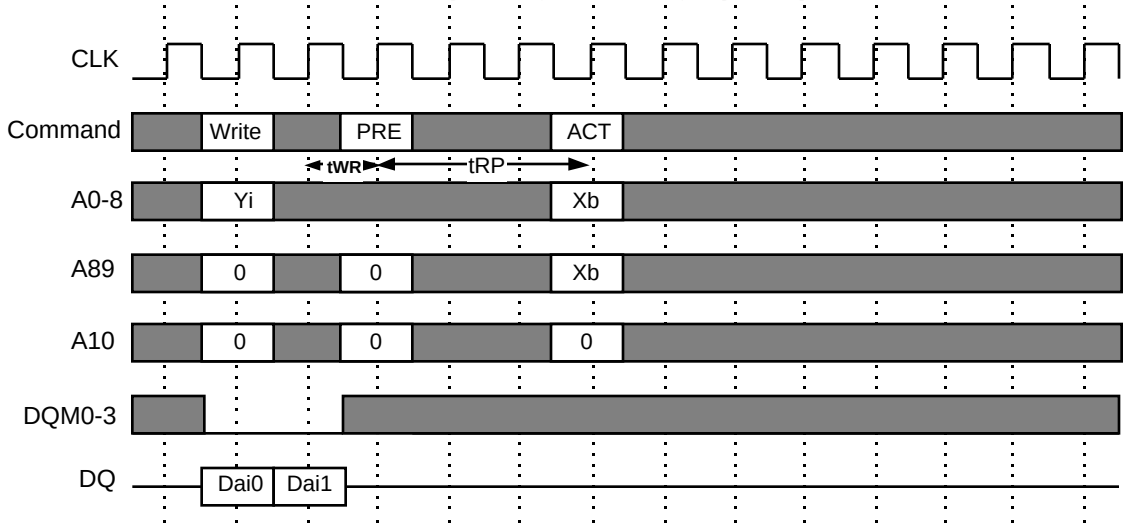
Write Interrupted by Read (BL=4, CL=3)



[Write Interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same bank. Random column access is allowed.

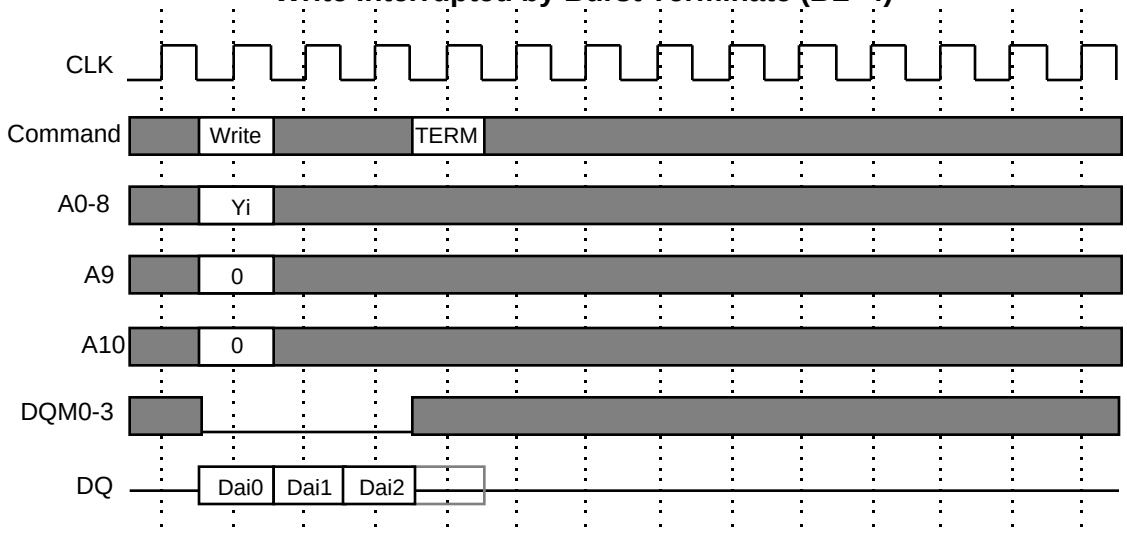
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

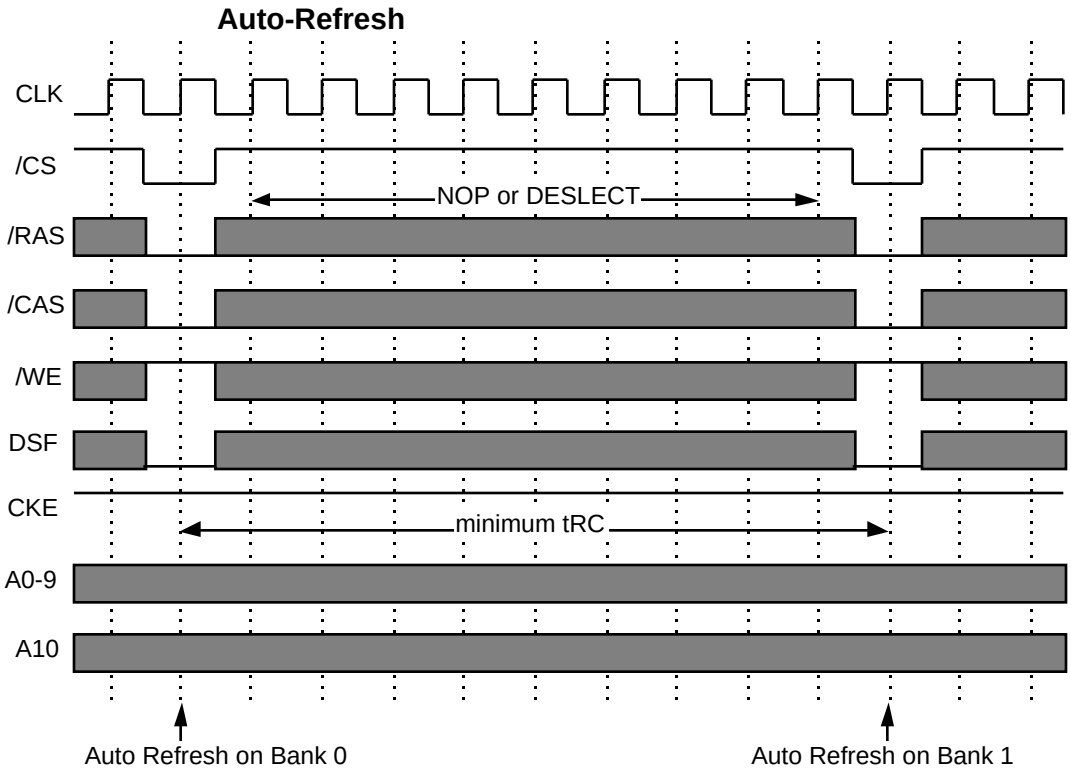
Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. The figure below shows the case that 3 words of data are written. Random column access is allowed. WRITE to TERM interval is minimum 1 CLK.

Write Interrupted by Burst Terminate (BL=4)



AUTO REFRESH

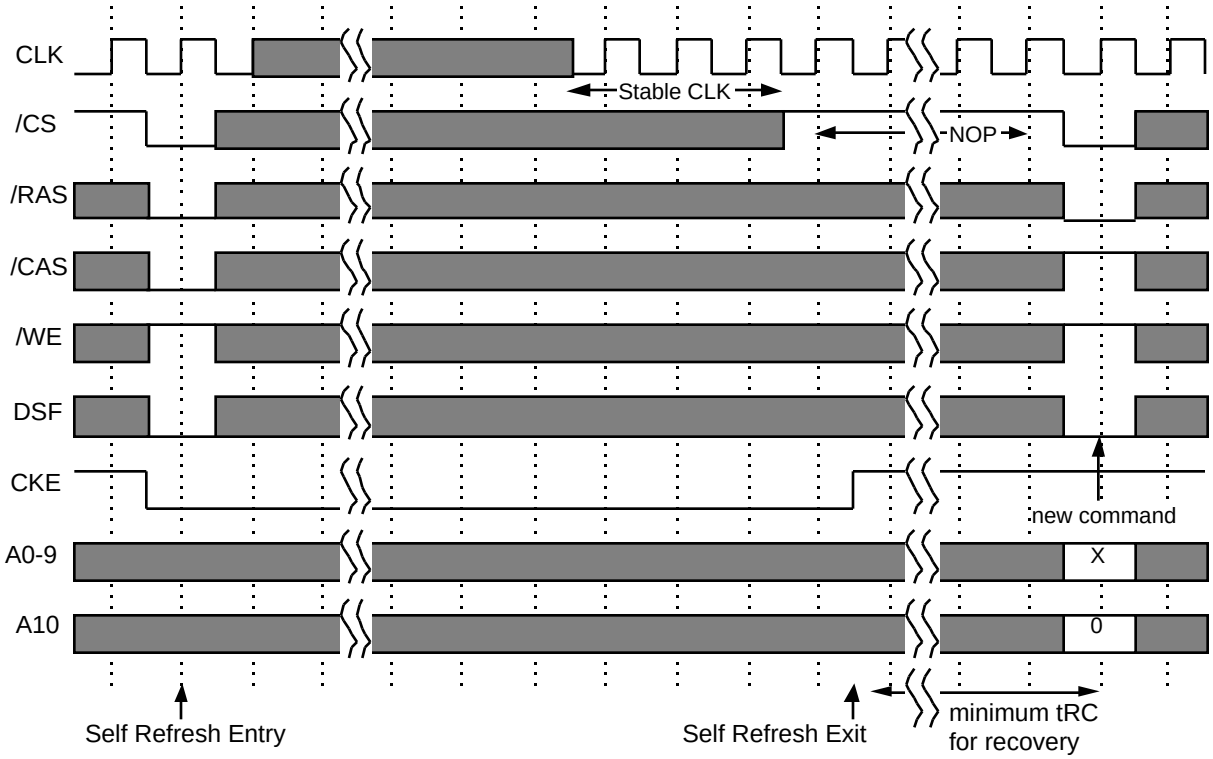
Single cycle of auto-refresh is initiated with REFA (/CS= /RAS= /CAS= DSF= L, /WE= /CKE= H) command. The refresh address is generated internally. 2048 REFA cycles within 32ms refresh 16Mbit memory cells. The auto-refresh is performed on each bank alternately (ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before tRC from the REFA command.



SELF REFRESH

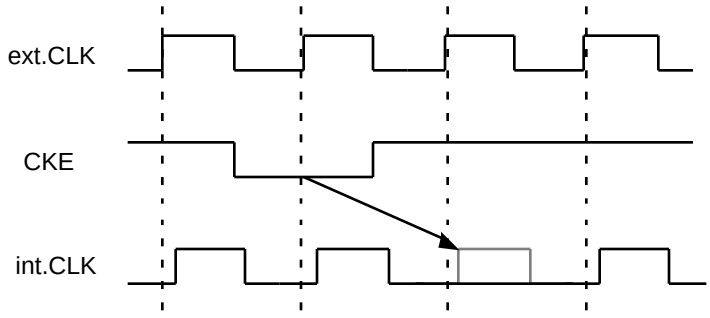
Self-refresh mode is entered by issuing a REFS command (/CS= /RAS= /CAS= DSF= L, /WE= H, CKE= L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input (but asynchronous), all other inputs including CLK are disabled and ignored, and power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE (REFSX). After tRC from REFSX both banks are in the idle state and a new command can be issued after tRC, but DESEL or NOP commands must be asserted until then.

Self-Refresh

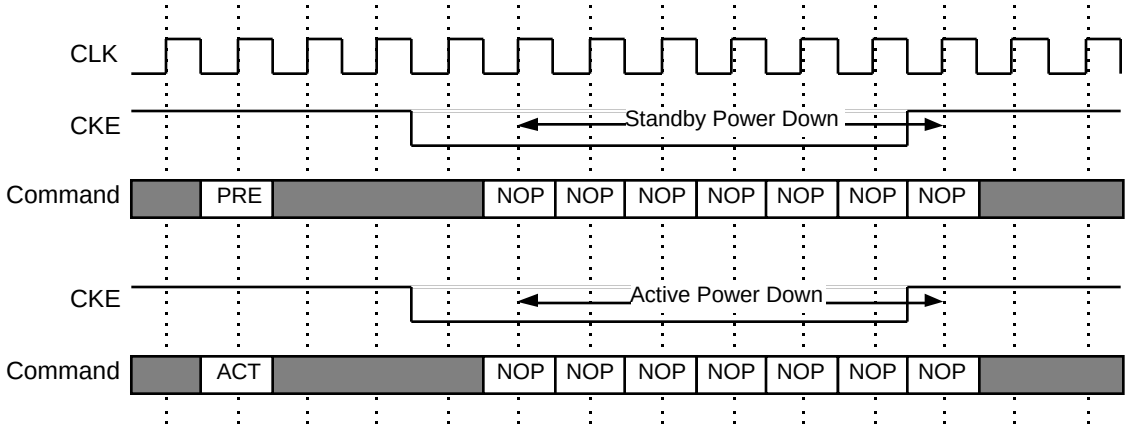


CLK SUSPEND

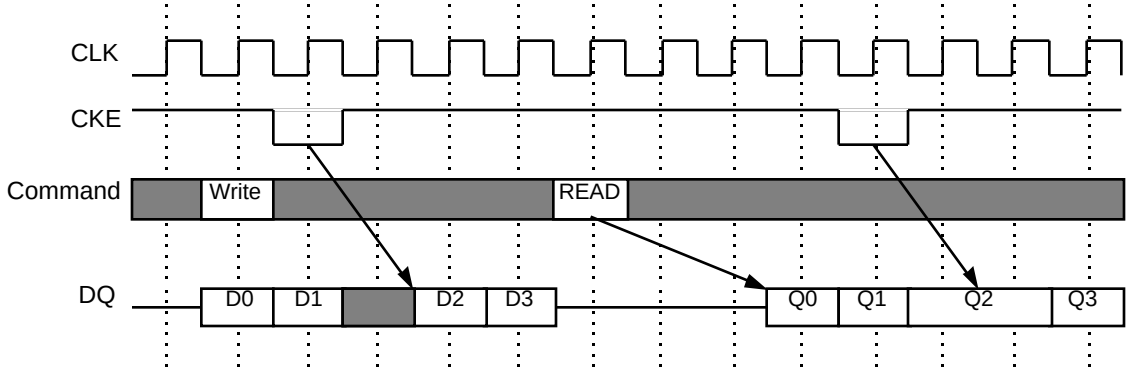
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.



Power Down by CKE



DQ Suspend by CKE



DQM0 - 3 CONTROL

DQM0 - 3 is a dual function signal defined as the data mask for writes and the output disable for reads.

During writes, DQM0 - 3 masks input data.

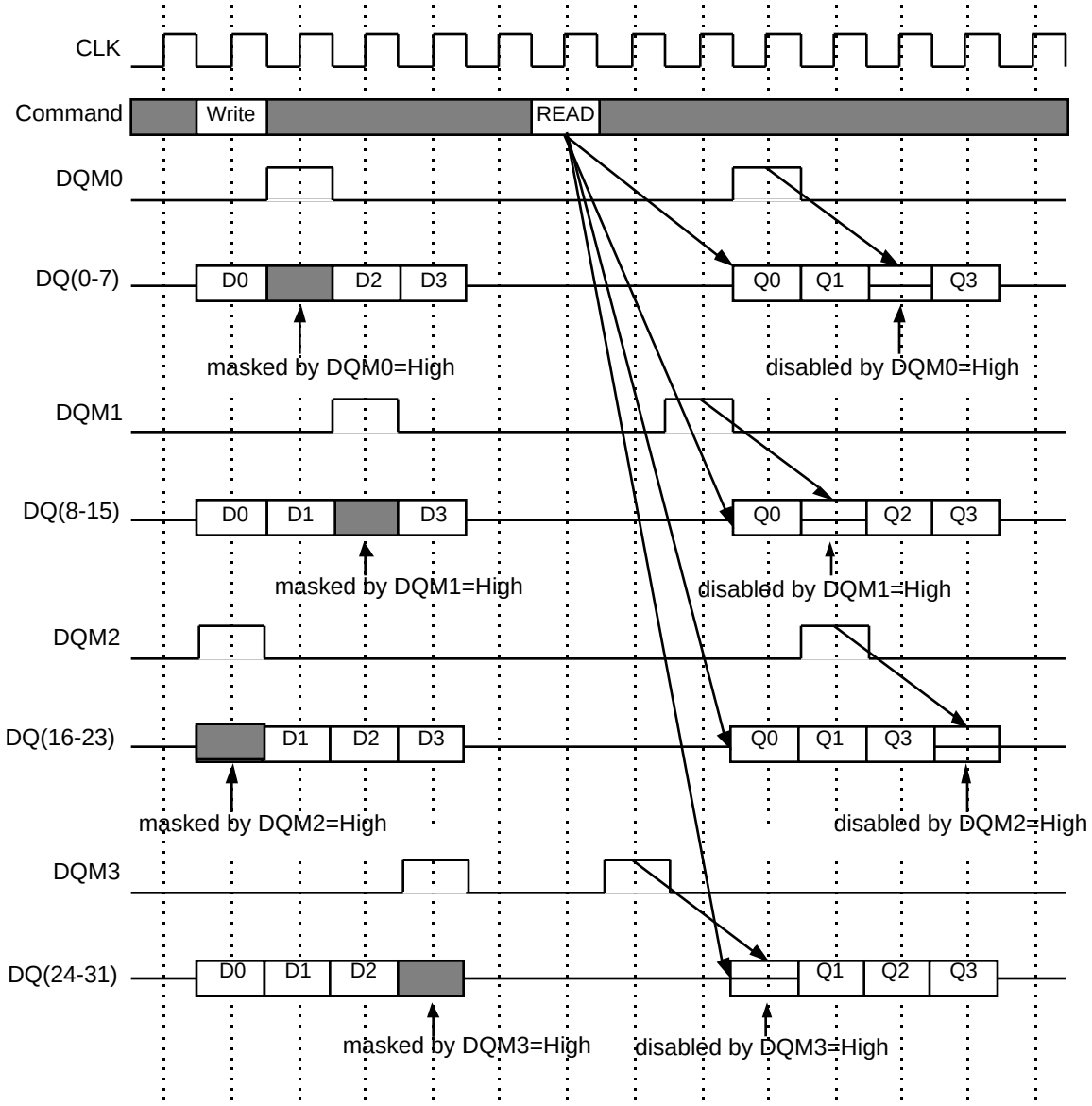
DQM0 - 3 to write mask latency is 0.

During reads, DQM0 - 3 forces output to Hi-Z.

DQM0 - 3 to output Hi-Z latency is 2.

DQM0 masks DQ0-7, DQM1 masks DQ8-15, DQM2 masks DQ16-23, DQM3 masks DQ24-031.

DQM0 - 3 Function



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 4.6	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 ~ 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 ~ 4.6	V
VO	Output Voltage	with respect to VssQ	-0.5 ~ 4.6	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25 °C	1000	mW
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-65 ~ 150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VddQ	Supply Voltage for Output	3.0	3.3	3.6	V
VssQ	Supply Voltage for Output	0	0	0	V
VIH*1	High-Level Input Voltage all inputs	2.0		VddQ+0.3	V
VIL*2	Low-Level Input Voltage all inputs	-0.3		0.8	V

NOTES:
1. VIH (max) = 5.5V for pulse width less than 10ns.
2. VIL (min) = -1.0V for pulse width less than 10ns.

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits (max.)	Unit
CI(A)	Input Capacitance, address pin	VI=Vss f=1MHz Vi=25mVrms	5	pF
CI(C)	Input Capacitance, control pin		5	pF
CI(K)	Input Capacitance, CLK pin		5	pF
CI/O	Input Capacitance, I/O pin		7	pF

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits(max)			Unit
			-8	-10	-12	
Icc1s*1	operating current, single bank	tRC=min, tCLK=min, BL=1, CL=3	TBD			mA
Icc1d*1	operating current, dual bank	tRC=min, tCLK=min, BL=1, CL=3	TBD			mA
Icc2h	standby current, CKE=H	both banks idle, tCLK=min, CKE=H	TBD			mA
Icc2l	standby current, CKE=L	both banks idle, tCLK=min, CKE=L	TBD			mA
Icc3	active standby current	both banks active, tCLK=min, CKE=H	TBD			mA
Icc4*1	burst current	tCLK=min, BL=4, CL=3, 1 bank idle	TBD			mA
Icc5	auto-refresh current	tRC=min, tCLK=min	TBD			mA
Icc6	self-refresh current	CKE <0.2v	TBD			mA
Icc7	operating current, block write	tCLK=min	TBD			mA

NOTES:
1. Icc (max) is specified at the output open condition.

AC OPERATING CONDITIONS AND CHARACTERISTICS

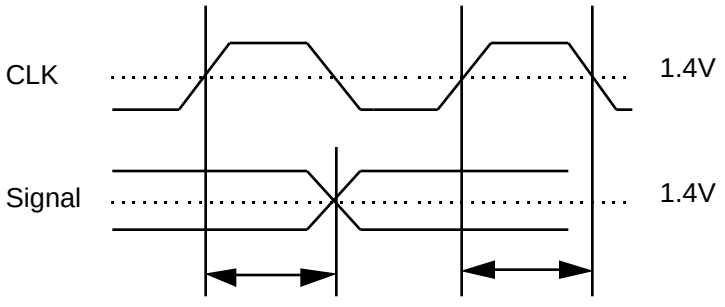
(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		Unit
			Min.	Max.	
VOH (DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL (DC)	Low-Level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating VO=0 ~ VddQ	-10	10	µA
I_I	Input Current	VIH = 0 ~ VddQ+0.3V	-10	10	µA

AC TIMING REQUIREMENTS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)
Input Pulse Levels : 0.8V to 2.0V
Input Timing Measurement Level : 1.4V

Symbol	Parameter		Limits						Unit
			-8		-10		-12		
			Min.	Max.	Min.	Max.	Min.	Max.	
tCLK	CLK cycle time	CL=2	12		15		18		ns
		CL=3	8		10		12		ns
tCH	CLK High pulse width		3		3.5		4		ns
tCL	CLK Low pulse width		3		3.5		4		ns
tT	Transition time of CLK		1	10	1	10	1	10	ns
tIS	Input Setup time (all inputs)		2.5		2.5		3		ns
tIH	Input Hold time (all inputs)		1		1		1.5		ns
tRC	Row Cycle time		96		100		120		ns
tRCD	Row to Column Delay		24		30		36		ns
tRAS	Row Active time		70	10000	70	10000	84	10000	ns
tRP	Row Precharge time		30		30		36		ns
tWR	Write Recovery time		8		10		12		ns
tRRD	Act to Act Delay time		30		30		36		ns
tRSC	Mode Register Set Cycle time		16		20		24		ns
tPDE	Power Down Exit time		8		12		15		ns
tREF	Refresh Interval time			32		32		32	ms
tBWC	Block Write Cycle time		16		20		24		ns
tBPL	Block Write to Precharge		8		10		12		ns



Any AC timing is referenced to the input signal crossing through 1.4V.

SWITCHING CHARACTERISTICS

(Ta=0 ~ 70°C, Vdd = VddQ = 3.3 ± 0.3v, Vss = VssQ = 0v, unless otherwise noted)

Symbol	Parameter		Limits						Unit
			-8		-10		-12		
			Min.	Max.	Min.	Max.	Min.	Max.	
tAC	Access time from CLK	CL=2		9		11		14	ns
		CL=3		7		8		10	ns
tOH	Output Hold time from CLK		3		3		3		ns
tOLZ	Delay time, output low impedance from CLK		0		0		0		ns
tOHZ	Delay time, output high impedance from CLK		3	7	3	8	3	8	ns

Output Load Condition