M52347SP/FP

SYNC SIGNAL PROCESSOR

DESCRIPTION

The M52347 automatically selects three types of synchronous signals containing separate sync (positive and negative polarities of 0.5 to 2.5 V_{P-P}), composite sync (positive and negative polarities of 0.5 to 2.5 V_{P-P}) and sync-on-video (sync negative polarity), and performs waveform shaping. The IC is optimum to synchronous signal processing for multi-scan type display monitor.

FEATURES

- Low power consumption with supply voltage of 5V
- Capable of obtaining output information on whether to input synchronous signal, and on polarity
- Output of clamp pulse
- Equipped with V TIME GATE SW that enables selecting whether or not VD portion pulse is output from pin ⑭/⑮.
- Equipped with CLAMP SW that enables switching the clamp pulse output position.

APPLICATION

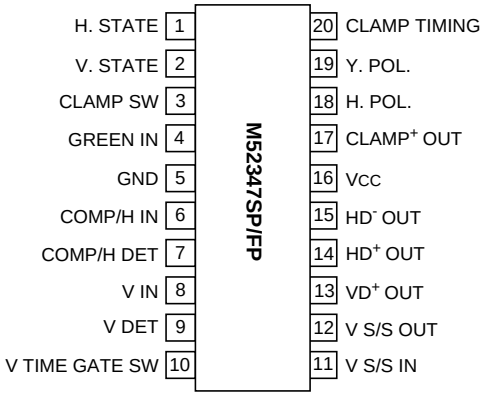
Display monitor

RECOMMENDED OPERATING CONDITION

Supply voltage range.....Vcc=4.5 to 5.5V

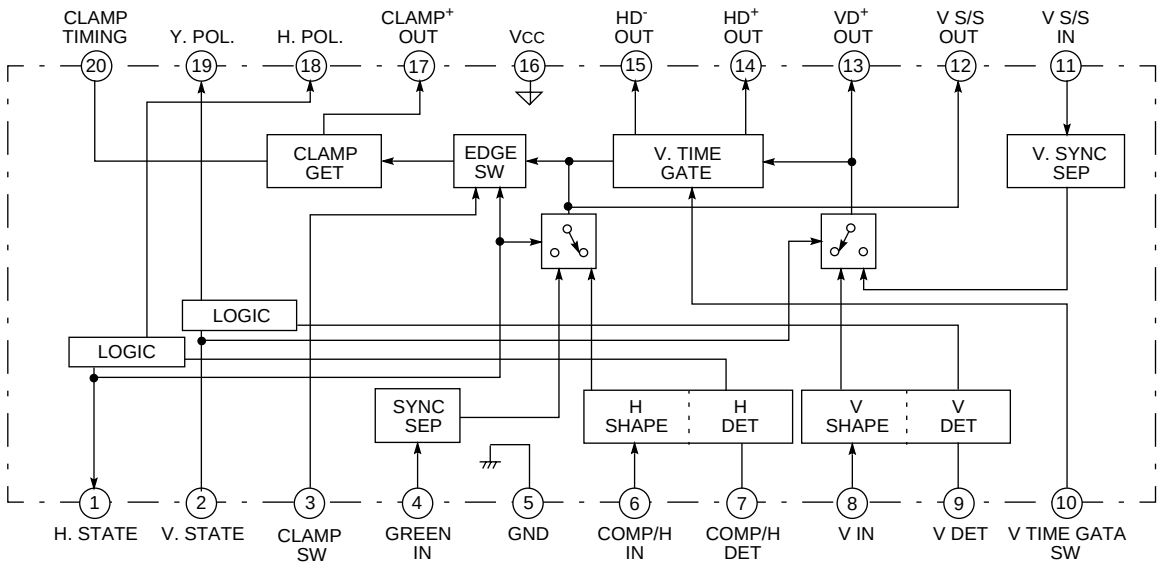
Rated Supply voltage.....Vcc=5V

PIN CONFIGURATION (TOP VIEW)



Outline 20P4B(SP)
20P2N-A(FP)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Ta=25˚C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	6.0	V
Pd	Power dissipation	1237.6(SP),827.8(FP)	mW
Surge	Electrostatic discharge	±200	V
T_{opr}	Operating temperature	-20 to +85	˚C
T_{stg}	Storage temperature	-40 to +150	˚C

ELECTRICAL CHARACTERISTICS (Ta=25˚C, Vcc=12V, unless otherwise noted)

Symbol	Parameter	Relay condition				TP condition		Input pin	Input condition	Output pin	Output waveform	Note	Limits			Unit
		4	6	8	16	3	10						Min.	Typ.	Max.	
Circuit current	I_{CC}	2	2	2	2	5V	5V	⑯		A			40	53	66	mA
1 OH	Pin①output Hi level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1VP-P; 1µS 50kHz 1VP-P	①	DC		4.0	5.0	5.0	V
1 OL	Pin①output Low level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 0.2VP-P; 1µS 50kHz 1.0VP-P	①	DC	0.2 V_{P-P} of input signal is equiv-alent to NON SYNC.	0	0.04	0.5	V
2 OH	Pin②output Hi level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1VP-P; 1µS 50kHz 1VP-P	②	DC		4.0	5.0	5.0	V
2 OL	Pin②output Low level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1.0VP-P; 1µS 50kHz 0.2VP-P	②	DC	0.2 V_{P-P} of input signal is equiv-alent to NON SYNC.	0	0.04	0.5	V
18 OH	Pin⑱output Hi level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1VP-P; 1µS 50kHz 1VP-P	⑱	DC		4.0	5.0	5.0	V
18 OL	Pin⑱output Low level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1VP-P; 1µS 50kHz 1VP-P	⑱	DC		0	0.04	0.5	V
19 OH	Pin⑲output Hi level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1VP-P; 1µS 50kHz 1VP-P	⑲	DC		4.0	5.0	5.0	V
19 OL	Pin⑲output Low level	2	1	1	1	0V 2.5V 5V	5V	⑥ ⑧	1µS 50kHz 1VP-P; 1µS 50kHz 1VP-P	⑲	DC		0	0.04	0.5	V
14 OH	Pin⑭output Hi level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P; 1µS 50kHz 2VP-P	⑭	- - -V Meas		4.0	5.0	5.0	V
14 OL	Pin⑭output Low level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P; 1µS 50kHz 2VP-P	⑭	- - -V Meas		0	0.25	0.5	V

The true value table depends on Table 1.

ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Relay condition				TP condition		In put pin	Input condition	Out put pin	Output waveform	Note	Limits			Unit
		4	6	8	16	3	10						Min.	Typ.	Max.	
15 OH	Pin⑮output Hi level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P 1µS 50kHz 2VP-P	⑮	- -V Meas		4.0	5.0	5.0	V
15 OL	Pin⑮output Low level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P 1µS 50kHz 2VP-P	⑮	- -V Meas		0	0.25	0.5	V
17 OH	Pin⑰output Hi level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P 1µS 50kHz 2VP-P	⑰	- -V Meas		4.0	5.0	5.0	V
17 OL	Pin⑰output Hi level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P 1µS 50kHz 2VP-P	⑰	- -V Meas		0	0.25	0.5	V
13 OH	Pin⑬output Hi level	2	2	1	1	0V 2.5V 5V	5V	⑧	1µS 50kHz 2VP-P	⑬	- -V Meas		4.0	5.0	5.0	V
13 OL	Pin⑬output Low level	2	2	1	1	0V 2.5V 5V	5V	⑧	1µS 50kHz 2VP-P	⑬	- -V Meas		0	0.25	0.5	V
12 OH	Pin⑫output Hi level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P 1µS 50kHz 2VP-P	⑫	- -V Meas		4.0	5.0	5.0	V
12 OL	Pin⑫output Low level	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1µS 50kHz 0.6VP-P 1µS 50kHz 2VP-P	⑫	- -V Meas		0	0.25	0.5	V
SS-NV	Sync-Sep Sync input signa Max. noise amplitude voltage	1	2	2	1	0V 2.5V 5V	5V	④	1µS 50kHz 0.05VP-P	⑭ ⑮ ⑰	No pulse must be output.	Must not operate when input amplitude is 0.05 VP-P or less. (Pseudo noise signal)	-	-	0.05	VP-P
SS-LV	Sync-Sep Sync input signal Min. amplitude voltage	1	2	2	1	0V 2.5V 5V	5V	④	1µS 50kHz 0.2VP-P	⑭ ⑰	50kHz No pulse must be output in this portion.	Must operate when the input amplitude is 0.2 VP-P or more.	0.2	-	-	VP-P
V3H	CLAMP SW Threshold voltage H	2	1	2	1	Variable	5V	③ ⑥	DC voltage must be applied. 1µS 50kHz 2VP-P	⑭ ⑰ ⑮		Checking output pulse for output with a voltage of 5 VDC applied, decrease the DC voltage and then measure the voltage when the output pulse is not output.	2.8	3.1	3.4	V
V3L	CLAMP SW Threshold voltage H Variable	2	1	2	1	Variable	5V	③ ⑥	DC voltage must be applied. 1µS 50kHz 2VP-P	⑭ ⑰ ⑮		Checking output pulse for output with a voltage of 0 VDC applied, increase the DC voltage and then measure the voltage when the output pulse is not output.	1.0	1.3	1.6	V
V10	V TIME GATE SW Threshold voltageVariable	2	1	1	1	0V 5V	Variable	⑥ ⑧ ⑩	1µS 50kHz 2VP-P 1µS 50kHz 2VP-P DC voltage must be applied.	⑭ ⑮		Checking output pulse for output with a voltage of 5 VDC applied, decrease the DC voltage and then measure the voltage when the output pulse becomes narrow.	2.0	2.5	3.0	V

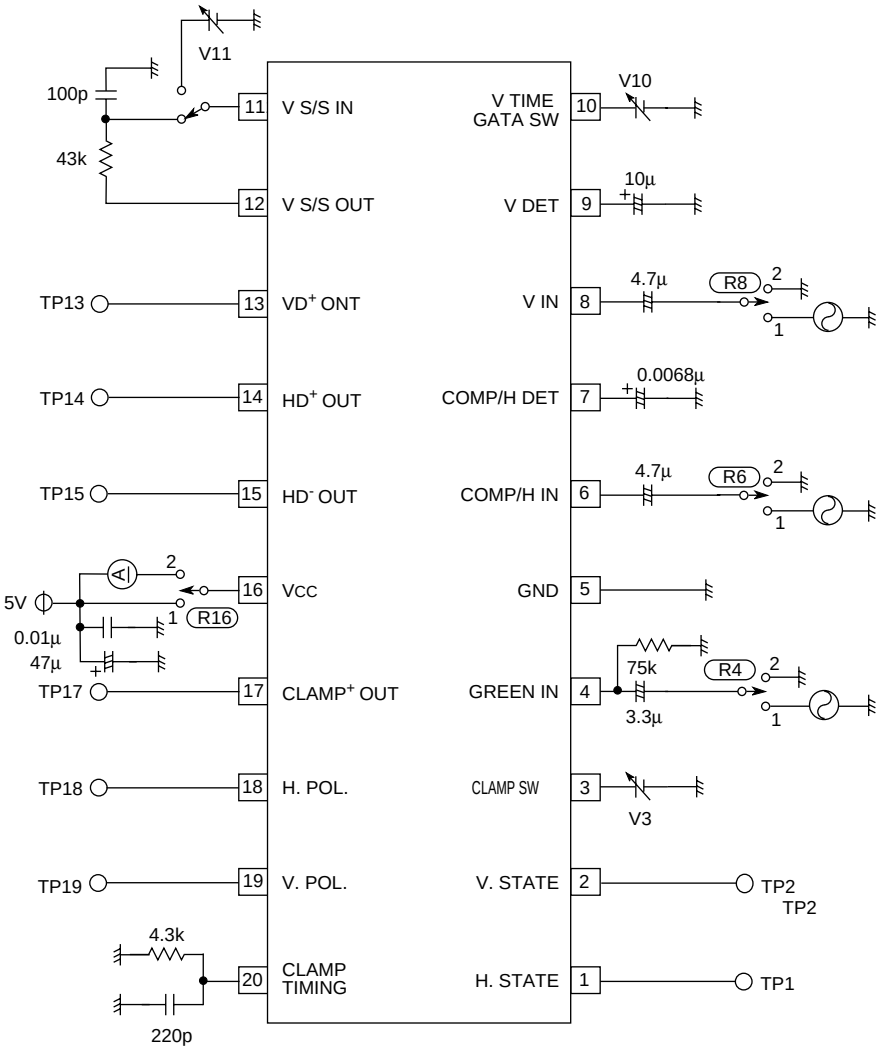
ELECTRICAL CHARACTERISTICS (cont.)

Symbol	Parameter	Relay condition				TP condition		In put pin	Input condition	Out put pin	Output waveform	Note	Limits			Unit
		4	6	8	16	3	10						Min.	Typ.	Max.	
HD^+-DA	HD^+-delay time (A)	1	1	2	1	0V 5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑭	Input ⑥ (50%) Time Meas Output ⑭ (50%)		-	120	350	nsec
HD^+-DB	HD^+-delay time (B)	1	1	2	1	0V 5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑭	Input ⑥ (50%) Time Meas Output ⑭ (50%)		-	80	350	nsec
HD^+-DC	HD^+-delay time (C)	1	1	2	1	2.5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑭	Input ④ (50%) Time Meas Output ⑭ (50%)		-	140	350	nsec
HD^+-DD	HD^+-delay time (D)	1	1	2	1	2.5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑭	nput ④ (50%) Time Meas Output ⑭ (50%)		-	120	350	nsec
HD^--DA	HD^--delay time (A)	1	1	2	1	0V 5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑮	nput ⑥ (50%) Time Meas Output ⑮ (50%)		-	70	350	nsec
HD^--DB	HD^--delay time (B)	1	1	2	1	0V 5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑮	nput ⑥ (50%) Time Meas Output ⑮ (50%)		-	120	350	nsec
HD^--DC	HD^--delay time (C)	1	1	2	1	2.5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑮	Input ④ (50%) Time Meas Output ⑮ (50%)		-	100	350	nsec
HD^--DD	HD^--delay time (D)	1	1	2	1	2.5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑮	Input ④ (50%) Time Meas Output ⑮ (50%)		-	150	350	nsec
CP^+-DA	CP^+-delay time (A)	1	1	2	1	0V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑰	nput ⑥ (50%) Time Meas Output ⑰ (50%)		-	90	350	nsec
CP^+-DB	CP^+-delay time (B)	1	1	2	1	2.5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑰	nput ④ (50%) Time Meas Output ⑰ (50%)		-	130	350	nsec
CP^+-DC	CP^+-delay time (C)	1	1	2	1	5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑰	nput ⑥ (50%) Time Meas Output ⑰ (50%)		-	90	350	nsec
CP^+-PW	CP^+-PULSE -WIDTH	1	1	2	1	0V 2.5V 5V	5V	④ ⑥	1μS 50kHz 0.6VP-P 1μS 50kHz 2VP-P	⑰	Time Meas Output ⑰ (50%)		250	400	550	nsec

ELECTRICAL CHARACTERISTICS (cont.)

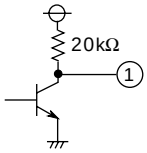
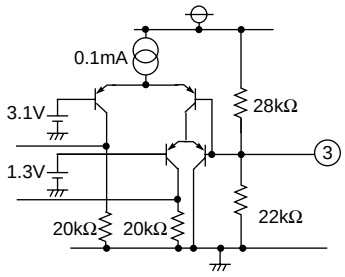
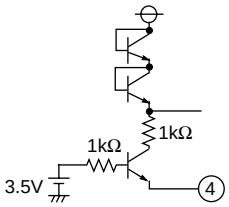
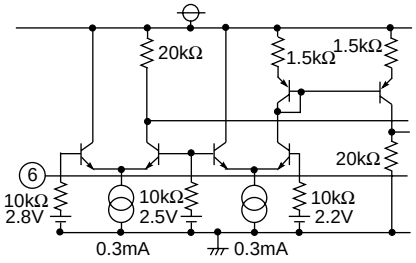
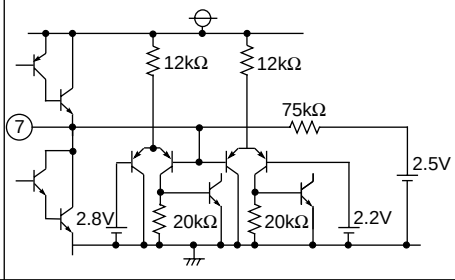
Symbol	Parameter	Relay condition				TP condition		In put pin	Input condition	Out put pin	Output waveform	Note	Limits			Unit
		4	6	8	16	3	10						Min.	Typ.	Max.	
VD^+-DA	VD^+ -delay time (A)	2	2	1	1	0V 2.5V 5V	5V	⑧	1µs 50kHz 2VP-P	⑬	Input ⑧ (50%) Time Meas Output ⑬ (50%)		-	100	350	nsec
VD^+-DB	VD^+ -delay time (B)	2	2	1	1	0V 2.5V 5V	5V	⑧	1µs 50kHz 2VP-P	⑬	Input ⑧ (50%) Time Meas Output ⑬ (50%)		-	70	350	nsec
V11H	V Sync-Sep Threshold voltage H	2	1	2	1	0V 5V	0V	⑥ ⑪	1µs 50kHz 2VP-P DC voltage must be applied.	⑭ ⑮		Checking output pulse for output with a voltage of 0 VDC applied, increase the DC voltage and then measure the voltage when the output pulse is not output.	3.0	3.5	4.0	V
V11L	V Sync-Sep Threshold voltage L	2	1	2	1	0V 5V	0V	⑥ ⑪	1µs 50kHz 2VP-P DC voltage must be applied.	⑭ ⑮		Checking output pulse for output with a voltage of 5 VDC applied, decrease the DC voltage and then measure the voltage when the output pulse is output.	1.3	1.8	2.3	V

TEST CIRCUIT



⊖ : 5V
Units Resistance : Ω
Capacitance : F

DESCRIPTION OF PIN

Pin No.	Name	Pin voltage	Peripheral circuit of pins	Description of function
①	H.STATE	0 VDC or 5 VDC		Logic output pin for horizontal synchronous signal When pin⑥input signal is POSI, outputs "H"; when NON, outputs "L"; and when NEG, outputs "H".
②	V.STATE	0 VDC or 5 VDC	Same as pin①	Logic output pin for vertical synchronous signal When pin⑧input signal is POSI, outputs "H"; when NON, outputs "L"; and when NEG, outputs "H".
③	CLAMP SW	≈2.2V when open		This SW is available to change the generating position of clamp pulse for input signal. (See Table 2.) VTH L =0 to1V VTH M =1.6 to 2.8V VTH H =3.4 to 5V
④	GREEN IN	≈2.8V when open		GREEN (SYNC ON VIDEO) input pin Input with negative sync. Comparison of pin④input signal and reference voltage within the IC performs synchronous separation.
⑤	GND			Grounding
⑥	COMP/H IN	≈2.5V when open		Composite sync/H sync input pin. Bias is approx. 2.5V and impedance is 10kΩ. The internal double threshold comparator is used for shaping waveform and detecting polarity. Optimum input amplitude is 0.6 Vp-p at pin⑥. Up to approx. 50% of duty, waveform shaping and polarity detection can be done.
⑦	COMP/H DET	≈2.5V when open (no signal)		External capacitance is required as a filter pin for detecting polarity and detecting non-input. As the value is larger, the ripple is smaller and less malfunction occurs. However, this lowers the response speed of detection.
⑧	V IN	≈2.5V when open	Same as pin⑥	V sync input pin Same as pin⑥
⑨	V DET	≈2.5V when open (no signal)	Same as pin⑦	Same as pin⑦

DESCRIPTION OF PIN (cont.)

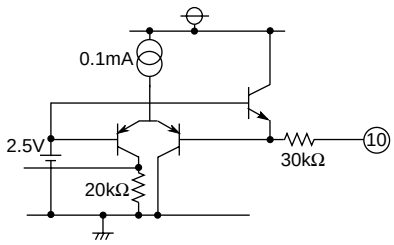
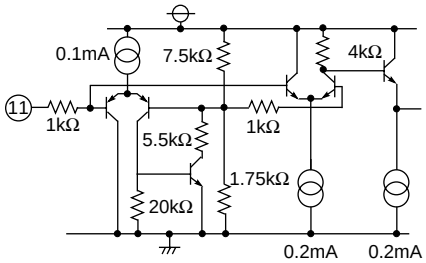
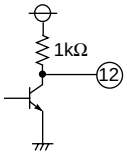
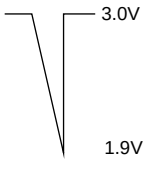
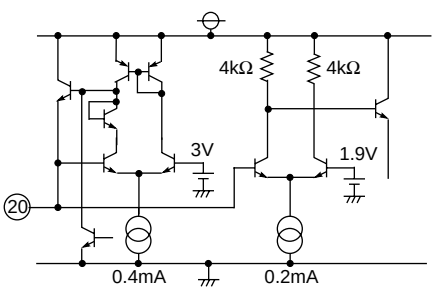
Pin No.	Name	Pin voltage	Peripheral circuit of pins	Description of function
⑩	V.TEME GATE SW	≈3.2V when open		V TIME GATE SW pin Can select whether to output the pulse of VD portion from pin ⑭,⑮ output pluse. The threshold voltage is approx. 2.5V. VTH L=0 to 2V VTH H=3 to 5V
⑪	V S/S IN			V S/S IN pin Inputs a signal of having externally integrated composite sync for V sync separation.
⑫	V S/S OUT			V S/S pulse output pin No problem occurs when current of approx. 6 mA flows to internal part of the IC. To improve the rising speed, connect a resistance between power supplies.
⑬	VD^+OUT		Same as pin⑫	VD^+ pulse output pin Same as pin ⑫
⑭	HD^+OUT		Same as pin⑫	HD^+ pulse output pin Same as pin ⑫
⑮	HD^-OUT		Same as pin⑫	HD^- pulse output pin Same as pin ⑫
⑯	VCC	5V		Power supply
⑰	$CLAMP^+$ OUT		Same as pin⑫	$CLAMP^+$ pulse output pin Same as pin ⑫
⑱	H.POL.	0 VDC or 5 VDC	Same as pin①	Logic output pin for horizontal synchronous signal When pin⑥input signal is POSI, outputs "L"; when NON, outputs "L"; and when NEG, outputs "H".
⑲	V.POL.	0 VDC or 5 VDC	Same as pin①	Logic output pin for vertical synchronous signal When pin⑧input signal is POSI, outputs "L"; when NON, outputs "L"; and when NEG, outputs "H".
⑳	CLAMP TIMING			CLAMP TIMING pin The clamp pulse width is determined depending on the external resistance and capacitance. As the resistance value and capacitance value are larger, the clamp pulse width is wider.

Table 1 DECODER Logic Output

Pin⑥input COMP/H	Pin⑧Input V	Output pin ①	②	⑱	⑲
POSI.	NON	H	L	L	L
	POSI.	H	H	L	L
	NEG.	H	H	L	H
NEG.	NON	H	L	H	L
	POSI.	H	H	H	L
	NEG.	H	H	H	H
NON.	NON	L	L	L	L
	POSI.	L	H	L	L
	NEG.	L	H	L	H

Table 2 Clamp Pulse Position

Input signal		Pin 17 output signal		
Pin ④	Pin ⑥	Pin③"H"	Pin③"M"	Pin③"L"
○	×	4 trailing edge	4 trailing edge	4 trailing edge
○	○	6 leading edge	4 trailing edge	6 trailing edge
×	○	6 leading edge	×	6 trailing edge

Table 3 Output Priority Order

Input signal			Output signal			
			Pin ③ "H" "L"		Pin③ "M"	
Pin ④	Pin ⑥	Pin ⑧	Pins ⑫,⑭,⑮,⑰	Pin ⑬	Pins ⑫,⑭,⑮,⑰	Pin ⑬
○	×	×	4	11	4	11
○	○	×	6	11	4	11
○	×	○	4	8	4	8
○	○	○	6	8	4	8
×	×	×	×	×	×	×
×	○	×	6	11	×	×
×	×	○	×	8	×	8
×	○	○	6	8	×	8

Table 4 Allowable Input Amplitude Voltage

Pin④input amplitude	VV 0 to 2.1(VP-P) VS 0.2 to 0.6(VP-P) fH=10Hz to 200kHz fV=10Hz to 200Hz
Pin⑥input amplitude	VS 0.5 to 2.5(VP-P) fH=10Hz to 200kHz
Pin⑧input amplitude	VS 0.5 to 2.5(VP-P) fV=10Hz to 200Hz

APPLICATION METHOD

1. Input block

1) GREEN (SYNC ON VIDEO) IN (Pin ③)

Input with sync negative polarity.

Comparison of pin ④ input signal and the reference voltage of the inside of the IC performs the synchronous separation. When the input at pin ④ is less than or equal to the reference voltage (2.8V) and the flowing current is more than or equal to the input sensitivity current (200 μ A or more), the signal is separated.

When only a synchronous signal is input into pin ④, the operatable amplitude and the duty are as shown in Figure 1.

If the IC does not operate normally with the video signal input, change the value of external resistance R to make the current optimum.

But, when capacity value is too big, output response becomes bad.

2) COMP/H IN, VIN (pins ⑥ and ⑧)

The composite sync input is connected to pin ⑥. H and V of the separate sync input are connected to pins ⑥ and ⑧, respectively. For each of pins ⑥ and ⑧, the bias is 2.5V and the impedance is 10 kΩ. The internal double threshold converter is used for shaping waveform and for detecting polarity.

Average DC voltage of input signal is 2.5V. Each threshold voltage is set at a voltage ±0.3V away from this voltage.

If the duty ratio at pin ⑥ is small as shown in Figure 2, the optimum value is approx. 0.3 V_{P-P}. If the duty ratio is large, the optimum value is approx. 0.6 V_{P-P}. Figure 3 shows the allowable input amplitude and the reference value of duty test.

Only 5V TTL input, decrease the amplitude by resistor splitting.

In addition, Figure 4 shows an example for improving the capability of the allowable duty when the input amplitude is 0.7 V_{P-P} or more.

To use the IC out of the standard value, remove the filter from pins ⑦ and ⑨, observe the waveform and check for a match with the waveform shown in Figure 5.

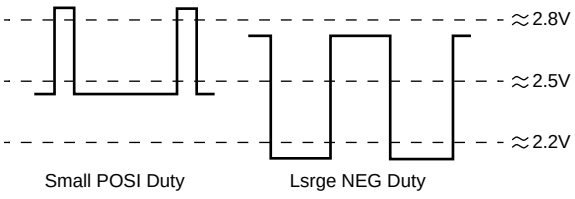


Fig. 2

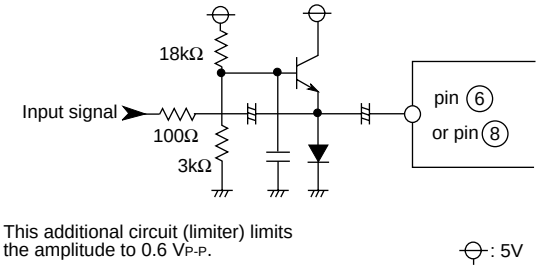


Fig. 4

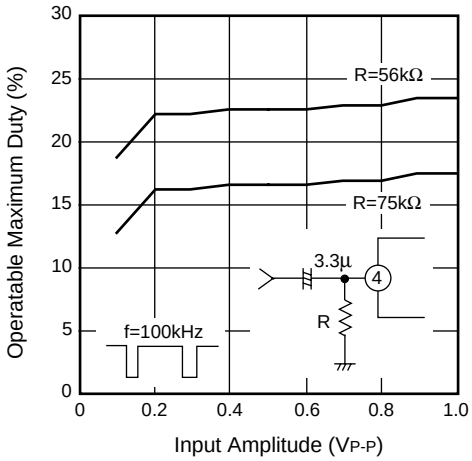


Fig. 1

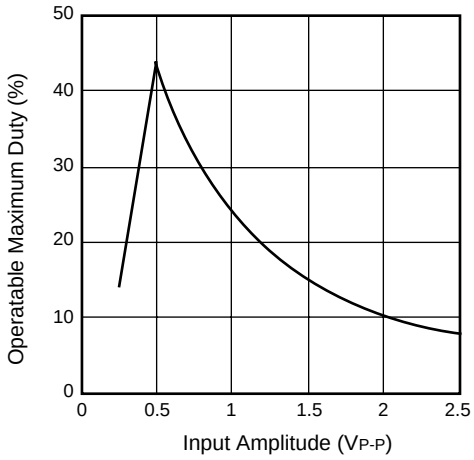


Fig. 3

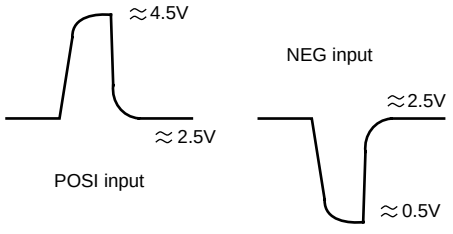


Fig. 5

3) Polarity detection and non-input detection (pins ⑦ and ⑧)

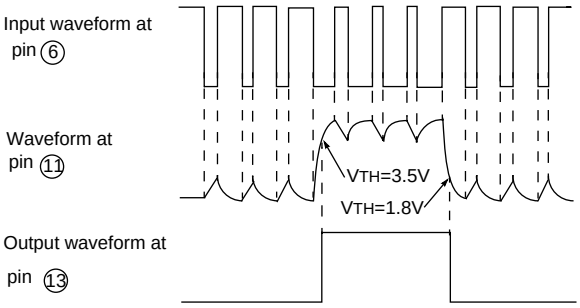
External capacitance is required as a filter pin to detect polarity and non-input. As the value is larger, the ripple is smaller and less malfunction occurs. However, the response speed for detection is lower. A sufficient external capacitance is 0.05 µF with input of 15 kHz and 10 uF with input of 60 kHz. However, check the frequency of the input signal in use and the filter pin waveform with the duty ratio conditions, and then check that the value is 3.1V or more (2.8V in capability) with positive polarity input and 1.9V or less (2.2V in capability) with negative polarity input.

4) V S/S IN (pin ⑪)

Input a signal of having externally integrated composite sync for V sync separation.

Composite sync input into pin ⑥ is output to pin ⑫. Output at ⑫ is externally integrated and is input into pin ⑪ for V sync separation. With the waveform at pin ⑪, check that the H element has been fully dropped.

The threshold levels of sync separation, given hysteresis, are 3.5V and 1.8V.



2. Clamp Pulse

1) Clamp pulse width

CLAMP TIMING (Pin ⑳)

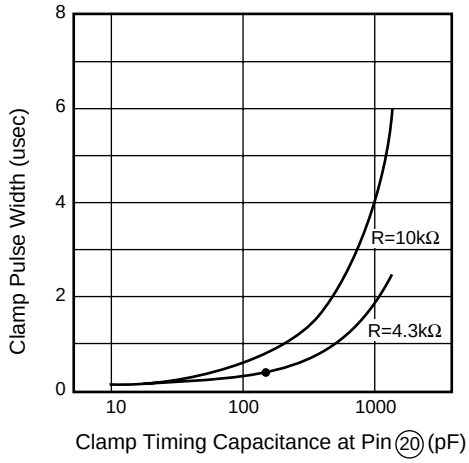
The clamp pulse width is determined by the external resistance and the capacitance. As the resistance value and capacitance value are larger, the clamp pulse width is wider.

The time constant is determined by the current flowing out of pin ⑳ and the capacitance value of the timing pin. The flow current at pin ⑳ is determined by the pin voltage and external resistance value. When the external resistance is 4.3 Ω (that is 700 uA) and the external capacitance is 220 pF, the pulse width is 0.4 usec.

2) Clamp pulse position

CLAMP SW (pin ③)

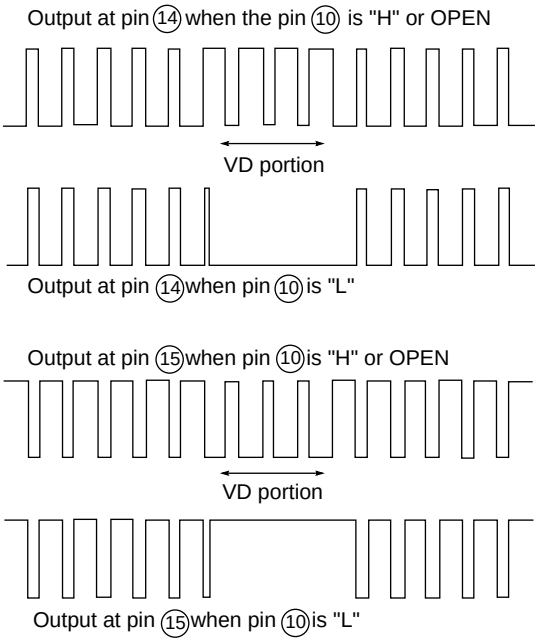
When pin ③ is "M" or "L", fixing a higher-priority signal to the trailing edge results in occurrence of a clamp pulse. When pin 3 is 'H", and only GREEN is input, clamp pulse occurs at the trailing edge. A clamp pulse also occurs at the leading edge when COMP/H only is input or when both COMP/H and GREEN are input.



3. Sampling Pulse from VD Portion

V TIME GATE SW (Pin ⑩)

Whether to output the pulse of VD portion from pins ⑭ and ⑮ can be selected. When pin ⑩ is "H" or OPEN, pulse of the VD portion is output. When pin ⑩ is "L", the pulse of the VD portion is not output.

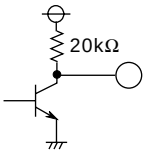


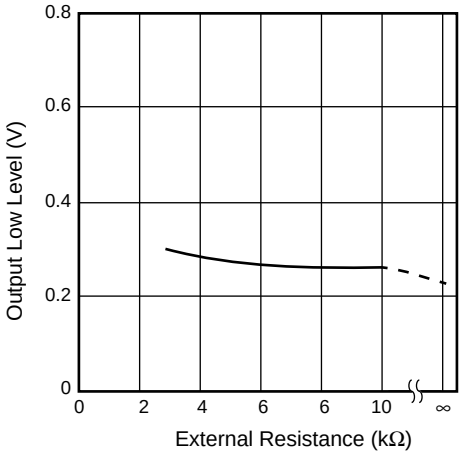
4. Output Stage

1) Logic output (pins ①, ②, ⑱ and ⑲)

The output format is as shown in the diagram below.

When the internal load resistance of the IC is 20 kΩ, a current of approx. 3 mA flows to the inside of the IC, no problem will occur.



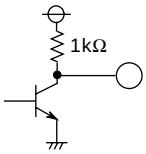


2) Pulse output (pins ⑫, ⑬, ⑭, ⑮,and ⑰)

The output format is as shown in the diagram below.

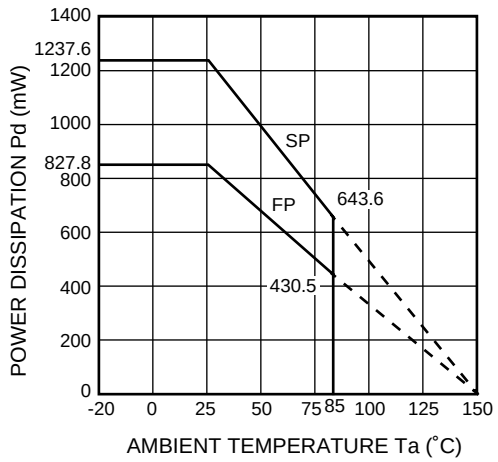
When the internal load resistance of the IC is 1 kΩ, a current of approx. 6 mA flows to the inside of the IC, no problem will occur.

To improve the rising speed, connect a resistance between power supplies. Note that the low level of the output pulse goes up.

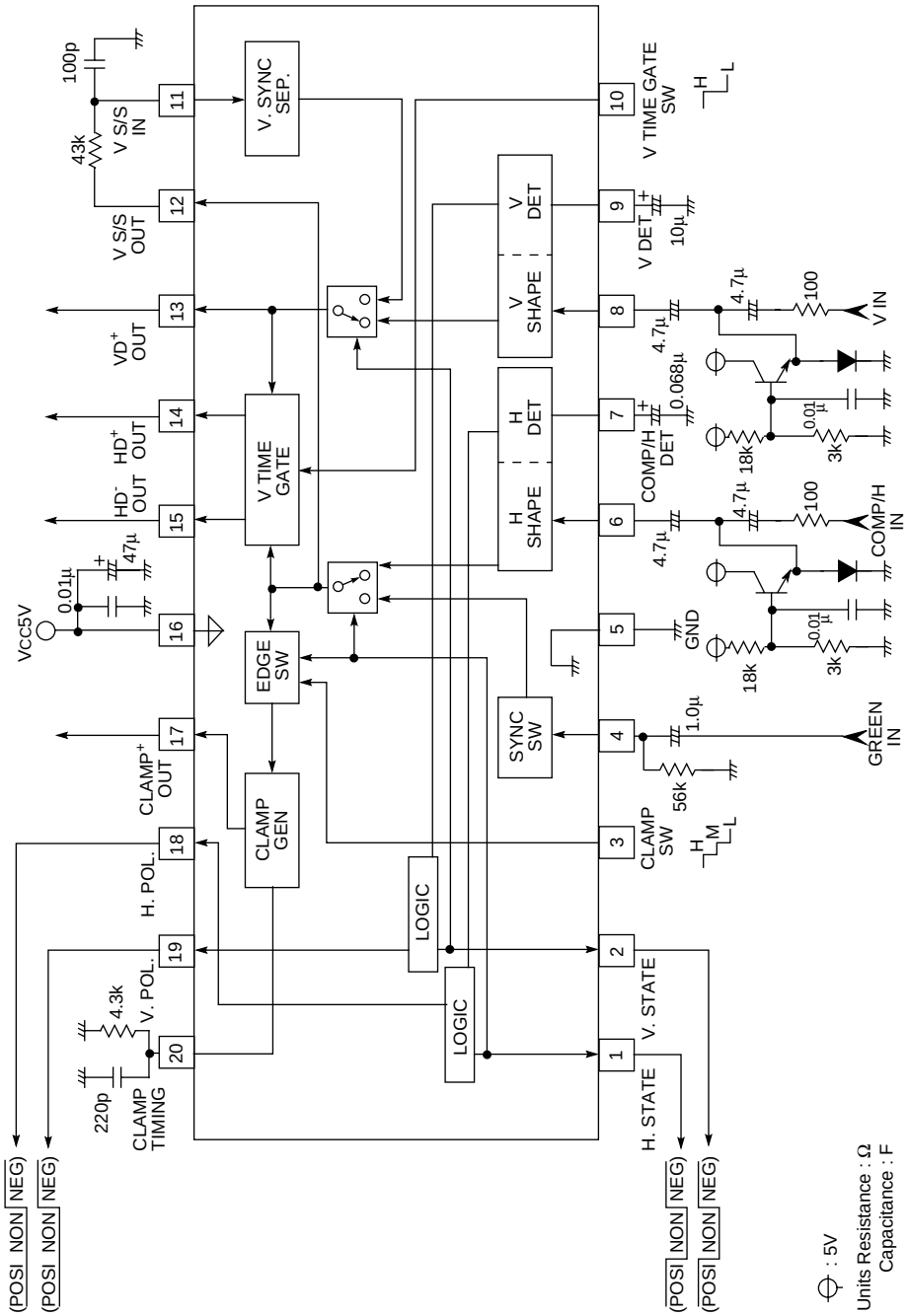


TYPICAL CHARACTERISTICS

THERMAL DERATING (MAXIMUM RATING)



APPLICATION EXAMPLE (f_H=50kHz, f_V=80 Hz)



* External circuit for input of pins 6 and 8
When amplitude of up to 5 V_{P-P} is entered into this circuit, can be kept constant at approx. 0.6 V_{P-P}.
When the duty of input signal at pins 6 and 8 changes, the most broad support range is obtained with ampl itude of 0.6 V_{P-P}.