

3-PHASE BRIDGE DRIVER

Features

- Floating channel designed for bootstrap operation
Fully operational to +600V or +1200V
Tolerant to negative transient voltage
dV/dt immune
- Gate drive supply range from 10V/12V to 20V DC and up to 25V for transient
- Undervoltage lockout for all channels
- Over-current shut down turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- 2.5V logic compatible
- Outputs out of phase with inputs
- Also available LEAD-FREE

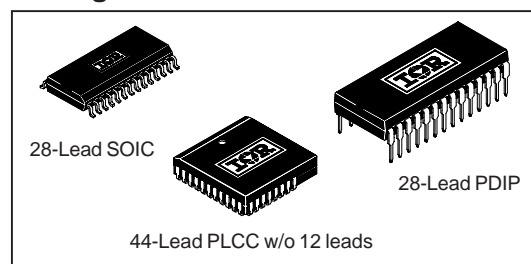
Description

The IR2133IR2135/IR2233IR2355 (J&S) are high voltage, high speed power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 2.5V logic. An independent operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs can also be derived from this resistor. A shutdown function is available to terminate all six outputs. An open drain FAULT signal is provided to indicate that an over-current or undervoltage shutdown has occurred. Fault conditions are cleared with the FLT-CLR lead. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channels can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts or 1200 volts.

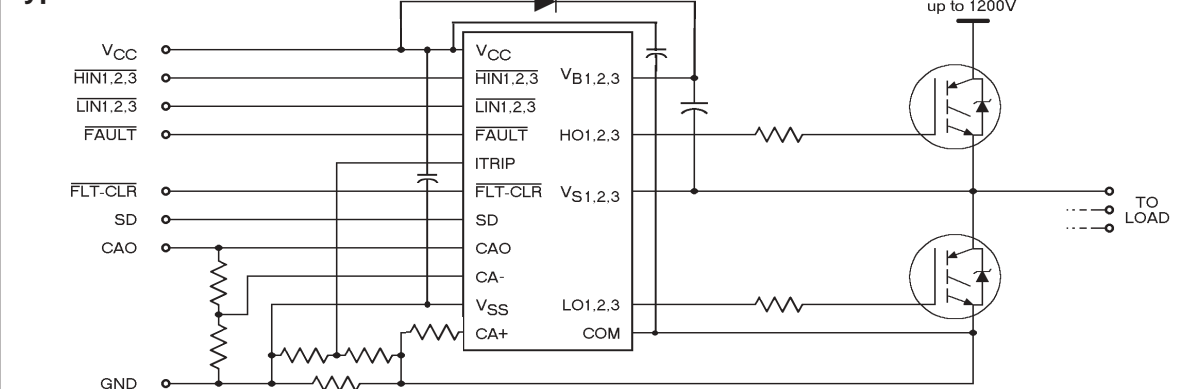
Product Summary

V_{OFFSET}	600V or 1200V max.
$I_{O+/-}$	200 mA / 420 mA
V_{OUT}	10 - 20V or 12 - 20V
$t_{on/off}$ (typ.)	750/700 ns
Deadtime (typ.)	250 ns

Packages



Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

IR2133/IR2135/IR2233/IR2235(J&S) & (PbF)

International
IR Rectifier

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
$V_{B1,2,3}$	High side floating supply voltage	(IR2133/IR2135)	-0.3	625	V
		(IR2233/IR2235)	-0.3	1225	
$V_{S1,2,3}$	High side floating supply offset voltage	$V_{B1,2,3} - 25$	$V_{B1,2,3} + 0.3$		
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3} - 0.3$	$V_{B1,2,3} + 0.3$		
V_{CC}	Fixed supply voltage	-0.3	25		
V_{SS}	Logic ground	$V_{CC} - 25$	$V_{CC} + 0.3$		
$V_{LO1,2,3}$	Low side output voltage	-0.3	$V_{CC} + 0.3$		
V_{IN}	Logic input voltage (HIN, LIN, ITRIP, SD & FLT-CLR)	$V_{SS} - 0.3$	($V_{SS} + 15$) or ($V_{CC} + 0.3$) whichever is lower		
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
$V_{OUT,AMP}$	Op amp output voltage (CAO)	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
V_{FLT}	FAULT output voltage	$V_{SS} - 0.3$	$V_{CC} + 0.3$		
dV_S/dt	Allowable offset supply voltage transient	—	50	V/ns	
P_D	Package power dissipation @ $T_A \leq 25^\circ\text{C}$	(28 Lead PDIP)	—	1.5	W
		(28 Lead SOIC)	—	1.6	
		(44 lead PLCC)	—	2.0	
R_{thJA}	Thermal resistance, junction to ambient	(28 Lead PDIP)	—	83	$^\circ\text{C/W}$
		(28 Lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T_J	Junction temperature	—	125	$^\circ\text{C}$	
T_S	Storage temperature	-55	150		
T_L	Lead temperature (soldering, 10 seconds)	—	300		

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The VS offset rating is tested with all supplies biased at 15V differential.

Symbol	Parameter Definition	Min.	Max.	Units	
$V_{B1,2,3}$	High side floating supply voltage	$V_{S1,2,3} + 10/12$	$V_{S1,2,3} + 20$	V	
$V_{S1,2,3}$	High side floating supply offset voltage	(IR2133/IR2135)	Note 1		600
		(IR2233/IR2235)	Note 1		1200
$V_{HO1,2,3}$	High side floating output voltage	$V_{S1,2,3}$	$V_{B1,2,3}$		
V_{CC}	Fixed supply voltage	10 or 12	20		
V_{SS}	Low side driver return	-5	5		
$V_{LO1,2,3}$	Low side output voltage	0	V_{CC}		
V_{IN}	Logic input voltage (HIN, LIN, ITRIP, SD & FLT-CLR)	V_{SS}	$V_{SS} + 5$		
$V_{IN,AMP}$	Op amp input voltage (CA+ & CA-)	V_{SS}	$V_{SS} + 5$		
$V_{OUT,AMP}$	Op amp output voltage (CAO)	V_{SS}	$V_{SS} + 5$		
V_{FLT}	FAULT output voltage	V_{SS}	V_{CC}		

Note 1: Logic operational for V_S of COM - 5V to COM + 600V/1200V. Logic state held for V_S of COM -5V to COM - V_{BS} . (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins, op amp input and output pins are internally clamped with a 5.2V zener diode.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V, $V_{S1,2,3}$ = V_{SS} , T_A = 25°C and C_L = 1000 pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	500	750	1000	ns	$V_{IN} = 0$ & 5V $V_{S1,2,3} = 0$ to 600V or 1200V
t_{off}	Turn-off propagation delay	450	700	950		
t_r	Turn-on rise time	—	90	150		
t_f	Turn-off fall time	—	40	70		
t_{sd}	SD to output shutdown propagation delay	500	750	1000		
t_{itrip}	ITRIP to output shutdown propagation delay	600	850	1100		
t_{bl}	ITRIP blanking time	—	400	—		
t_{flt}	ITRIP to \overline{FAULT} propagation delay	400	650	900		
$t_{fil,in}$	Input filter time (\overline{HIN} , \overline{LIN} and SD)	—	310	—		
t_{fltclr}	FLT-CLR to \overline{FAULT} clear time	600	850	1100		
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on	100	250	400	V/ μ s	$V_{IN} = 0$ & 5V
SR+	Amplifier slew rate (positive)	5	10	—		
SR-	Amplifier slew rate (negative)	2	2.5	—		

NOTE: For high side PWM, \overline{HIN} pulse width must be $\geq 1\mu$ sec

Static Electrical Characteristics

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V unless otherwise specified and T_A = 25°C. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels ($H_{S1,2,3}$ & $L_{S1,2,3}$). The V_O and I_O parameters are referenced to V_{SS} and $V_{S1,2,3}$ and are applicable to the respective output leads: $H_{O1,2,3}$ or $L_{O1,2,3}$.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "0" Input Voltage (OUT = LO)	2.2	—	—	V	
V_{IL}	Logic "1" Input Voltage (OUT = HI)	—	—	0.8		
$V_{FCLR,IH}$	Logic "0" Fault Clear Input Voltage	2.2	—	—		
$V_{FCLR,IL}$	Logic "1" Fault Clear Input Voltage	—	—	0.8		
$V_{SD,TH+}$	SD Input Positive Going Threshold	1.6	1.9	2.2		
$V_{SD,TH-}$	SD Input Negative Going Threshold	1.4	1.7	2.0		
$V_{IT,TH+}$	I_{TRIP} Input Positive Going Threshold	470	570	670	mV	
$V_{IT,TH-}$	I_{TRIP} Input Negative Going Threshold	360	460	560		
V_{OH}	High Level Output Voltage, $V_{BIAS} - V_O$	—	—	100	mV	$V_{IN} = 0V$, $I_O = 0A$
V_{OL}	Low Level Output Voltage, V_O	—	—	100		$V_{IN} = 5V$, $I_O = 0A$
I_{LK}	Offset Supply Leakage Current (IR2133/IR2135) (IR2233/IR2235)	—	—	50	μ A	$V_{B1,2,3}=V_{S1,2,3} = 600V$
		—	—	50		$V_{B1,2,3}=V_{S1,2,3} = 1200V$
I_{QBS}	Quiescent V_{BS} Supply Current	—	50	100	mA	$V_{IN} = 0V$ or 5V
I_{QCC}	Quiescent V_{CC} Supply Current	—	4	8		$V_{IN} = 0V$ or 5V
I_{IN+}	Logic "1" Input Bias Current (OUT = HI)	—	200	350	μ A	$V_{IN} = 0V$
I_{IN-}	Logic "0" Input Bias Current (OUT = LO)	—	100	250		$V_{IN} = 5V$
I_{SD+}	"High" Shutdown Bias Current	—	30	100	nA	SD = 5V
I_{SD-}	"Low" Shutdown Bias Current	—	—	100		SD = 0V
I_{ITRIP+}	"High" I_{TRIP} Bias Current	—	30	100	μ A	$I_{TRIP} = 5V$
I_{ITRIP-}	"Low" I_{TRIP} Bias Current	—	—	100	nA	$I_{TRIP} = 0V$

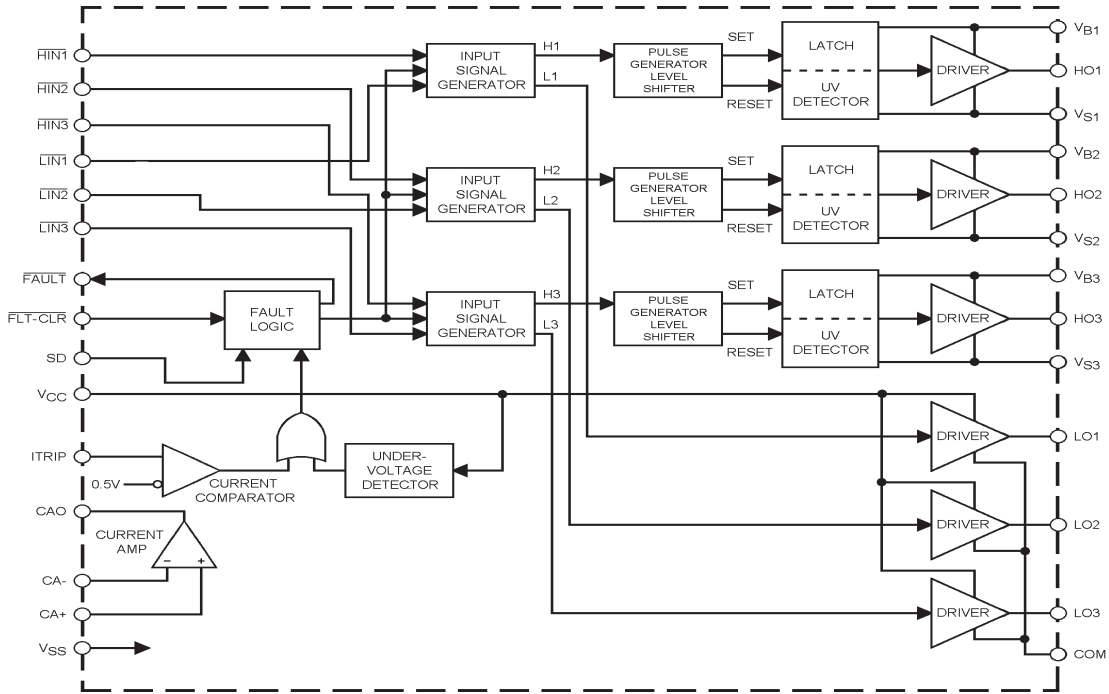
IR2133/IR2135/IR2233/IR2235(J&S) & (PbF)

Static Electrical Characteristics — Continued

V_{BIAS} (V_{CC} , $V_{BS1,2,3}$) = 15V and T_A = 25°C unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The V_O and I_O parameters are referenced to V_{SS} and $V_{S0,1,2,3}$ and are applicable to the respective output leads: HO or LO.

Symbol	Parameter Definition	Min.	Typ.	Max.	Units	Test Conditions
$I_{FLTCLR+}$	"High" Fault Clear Input Bias Current	—	200	350	μA	$\overline{FLT-CLR} = 0V$
$I_{FLTCLR-}$	"Low" Fault Clear Input Bias Current	—	100	250		$\overline{FLT-CLR} = 5V$
V_{BSUV+}	V _{BS} Supply Undervoltage Positive Going Threshold (for IR2133/IR2233)	7.6	8.6	9.6	V	
		(for IR2135/IR2235)	9.2	10.4		
V_{BSUV-}	V _{BS} Supply Undervoltage Negative Going Threshold (for IR2133/IR2233)	7.2	8.2	9.2		
		(for IR2135/IR2235)	8.3	9.4		
V_{BSUVH}	V _{BS} Supply Undervoltage Lockout Hysteresis (for IR2133/IR2233)	—	0.4	—		
		(for IR2135/IR2235)	—	1		
V_{CCUV+}	V _{CC} Supply Undervoltage Positive Going Threshold (for IR2133/IR2233)	7.6	8.6	9.6		
		(for IR2135/IR2235)	9.2	10.4		
V_{CCUV-}	V _{CC} Supply Undervoltage Negative Going Threshold (for IR2133/IR2233)	7.2	8.2	9.2		
		(for IR2135/IR2235)	8.3	9.4		
V_{CCUVH}	V _{CC} Supply Undervoltage Lockout Hysteresis (for IR2133/IR2233)	—	0.4	—		
		(for IR2135/IR2235)	—	1		
$R_{on,FLT}$	FAULT- Low On Resistance	—	70	100	Ω	
I_{O+}	Output High Short Circuit Pulsed Current	190	250	—	mA	$V_{OUT} = 0V$, $V_{IN} = 0V$ $PW \leq 10 \mu s$
I_{O-}	Output Low Short Circuit Pulsed Current	380	500	—		$V_{OUT} = 15V$, $V_{IN} = 5V$ $PW \leq 10 \mu s$
V_{OS}	Amplifier Input Offset Voltage	—	0	30	mV	$CA+ = 0.2V$, $CA- = CAO$
$I_{IN,AMP}$	Amplifier Input Bias Current	—	—	4	nA	$CA+ = CA- = 2.5V$
CMRR	Amplifier Common Mode Rejection Ratio	50	70	—		$CA+ = 0.1V$ & $5V$, $CA- = CAO$
PSRR	Amplifier Power Supply Rejection Ratio	50	70	—	dB	$CA+ = 0.2V$, $CA- = CAO$ $V_{CC} = 10V$ & $20V$
$V_{OH,Amp}$	Amplifier High Level Output Voltage	5	5.2	5.4	V	$CA+ = 1V$, $CA- = 0V$
$V_{OL,Amp}$	Amplifier Low Level Output Voltage	—	—	20	mV	$CA+ = 0V$, $CA- = 1V$
$I_{SRC,Amp}$	Amplifier Output Source Current	4	7	—	mA	$CA+ = 1V$, $CA- = 0V$, $CAO = 4V$
$I_{SNK,Amp}$	Amplifier Output Sink Current	0.5	1	—		$CA+ = 0V$, $CA- = 1V$, $CAO = 2V$
$I_{O+,Amp}$	Amplifier Output High Short Circuit Current	—	10	—		$CA+ = 5V$, $CA- = 0V$, $CAO = 0V$
$I_{O-,Amp}$	Amplifier Output Low Short Circuit Current	—	4	—		$CA+ = 0V$, $CA- = 5V$, $CAO = 5V$

Functional Block Diagram



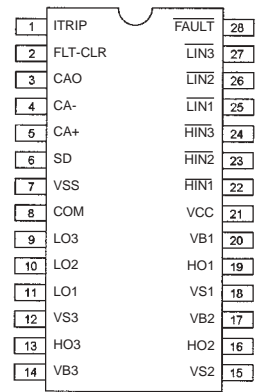
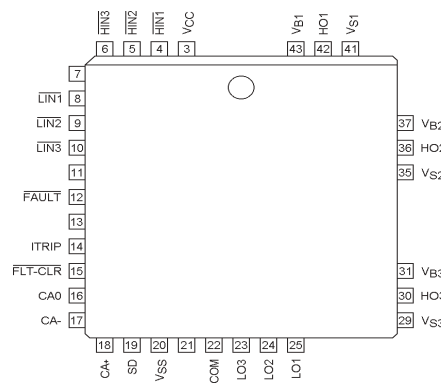
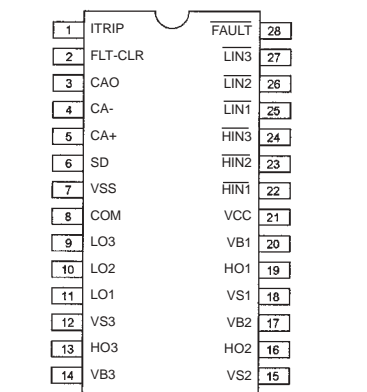
Lead Definitions

Symbol	Lead Description
$\overline{HIN1,2,3}$	Logic inputs for high side gate driver outputs (HO1,2,3), out of phase.
$\overline{LIN1,2,3}$	Logic inputs for low side gate driver outputs (LO1,2,3), out of phase.
\overline{FAULT}	Indicates over-current or undervoltage lockout (low side) has occurred, negative logic.
Vcc	Logic and low side fixed supply.
ITRIP	Input for over-current shut down.
$\overline{FLT-CLR}$	Logic input for fault clear, negative logic.
SD	Logic input for shut down.
CAO	Output of current amplifier.
CA-	Negative input of current amplifier.
CA+	Positive input of current amplifier.
Vss	Logic ground.
COM	Low side return.
VB1,2,3	High side floating supplies.
HO1,2,3	High side gate drive outputs.
VS1,2,3	High side floating supply returns.
LO1,2,3	Low side gate drive outputs

IR2133/IR2135/IR2233/IR2235(J&S) & (PbF)



Lead Assignments

 <p>28 Lead DIP</p>	 <p>44 Lead PLCC w/o 12 Leads</p>	 <p>28 Lead SOIC (Wide Body)</p>
<p>IR2133 IR2135 IR2233 IR2235</p>	<p>IR2133J IR2135J IR2233J IR2235J</p>	<p>IR2133S IR2135S IR2233S IR2235S</p>
<p>Part Number</p>		

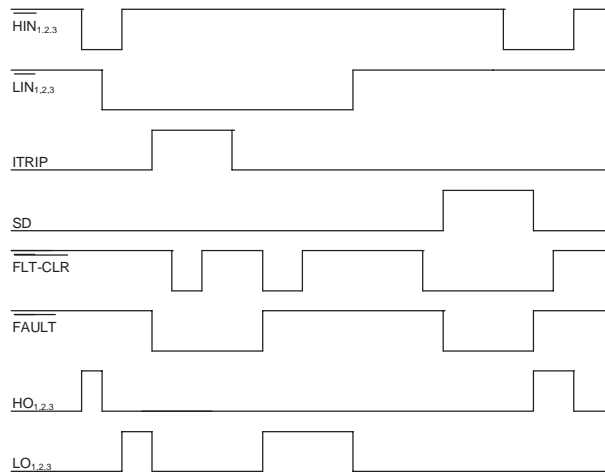


Figure 1. Input/Output Timing Diagram

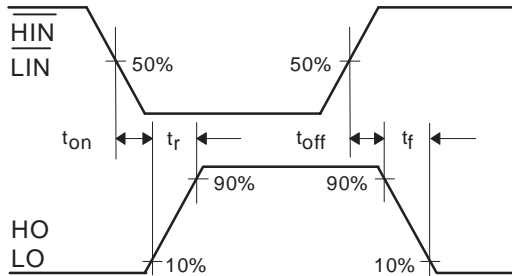


Figure 2. Switching Time Waveform Definitions

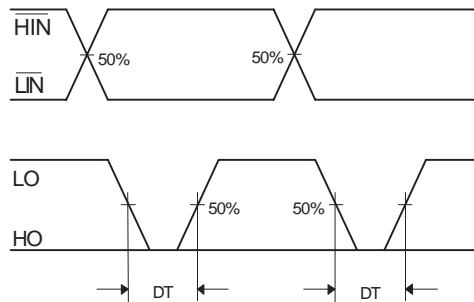


Figure 3. Deadtime Waveform Definitions

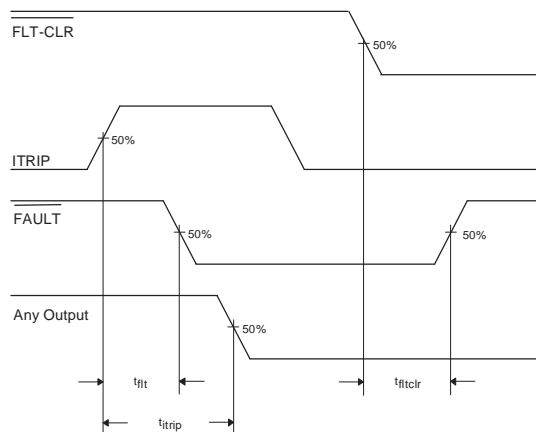


Figure 4. Overcurrent Shutdown Waveform

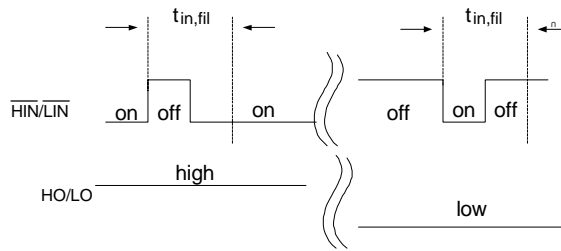


Figure 4.5 Input Filter Function

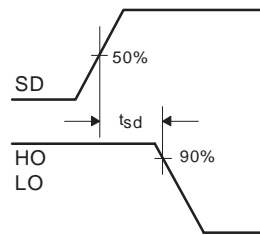


Figure 5. Shutdown Waveform Definitions

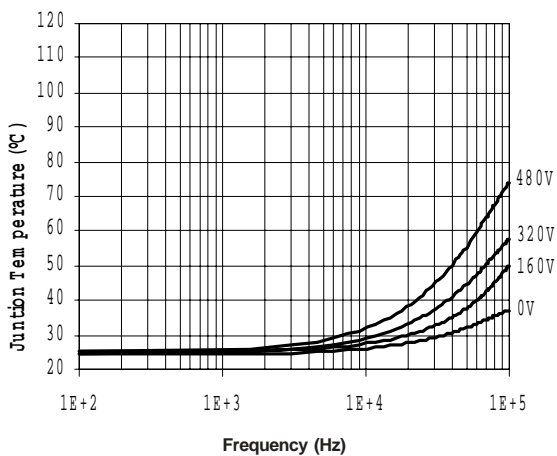


Figure 7. IR2133J Junction Temperature vs Frequency Driving (IRGPC20KD2) Rgate = 5.1Ω @ Vcc = 15V

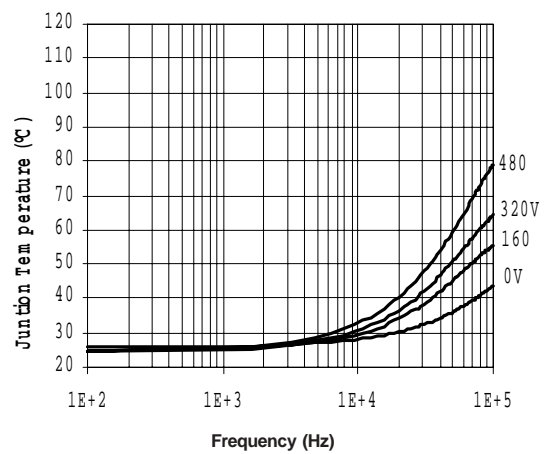


Figure 8. IR2133J Junction Temperature vs Frequency Driving (IRGPC30KD2) Rgate = 5.1Ω @ Vcc = 15V

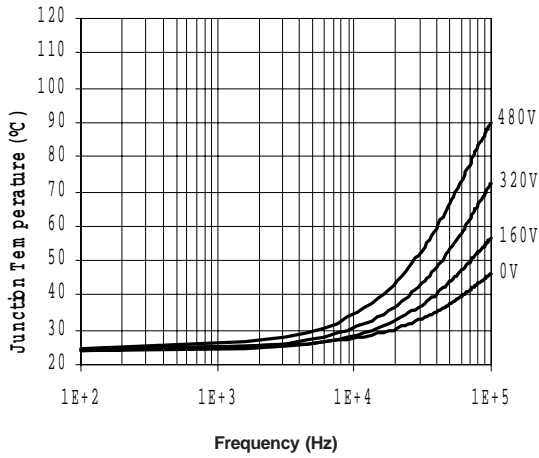


Figure 9. IR2133J Junction Temperature vs Frequency Driving (IRGPC40KD2) Rgate = 5.1Ω @ Vcc = 15V

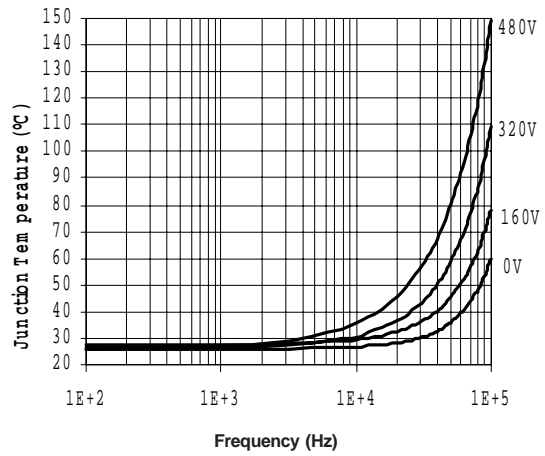


Figure 10. IR2133J Junction Temperature vs Frequency Driving (IRGPC50KD2) Rgate = 5.1Ω @ Vcc = 15V

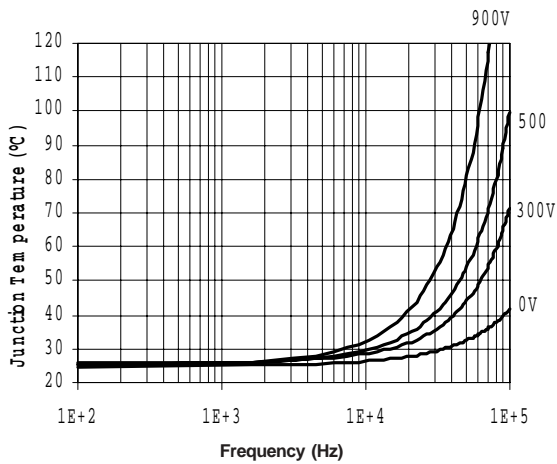


Figure 11. IR2233J Junction Temperature vs Frequency Driving (IRG4PH30KD) Rgate = 20Ω @ Vcc = 15V

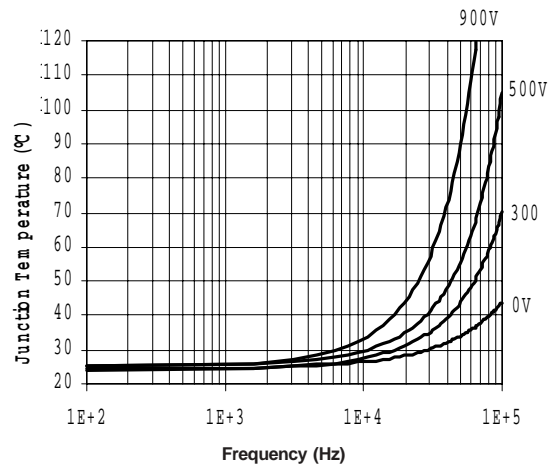


Figure 12. IR2233J Junction Temperature vs Frequency Driving (IRG4PH40KD) Rgate = 15Ω @ Vcc = 15V

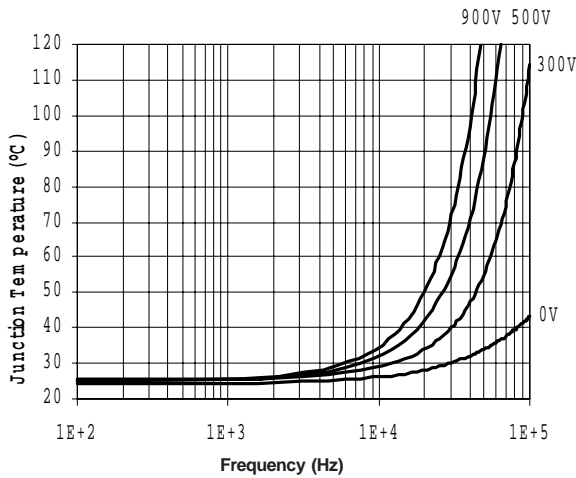


Figure 13. IR2233J Junction Temperature vs Frequency Driving (IRG4PH50KD) Rgate = 10Ω @ Vcc = 15V

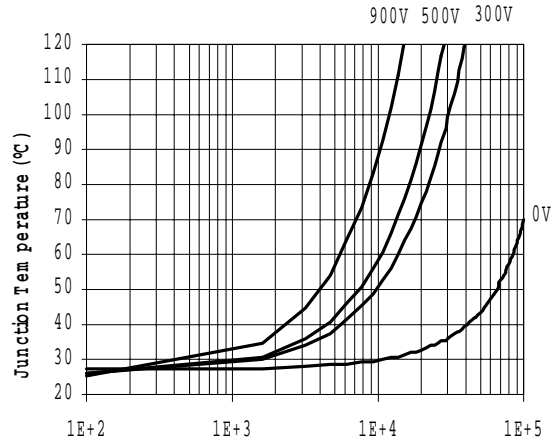
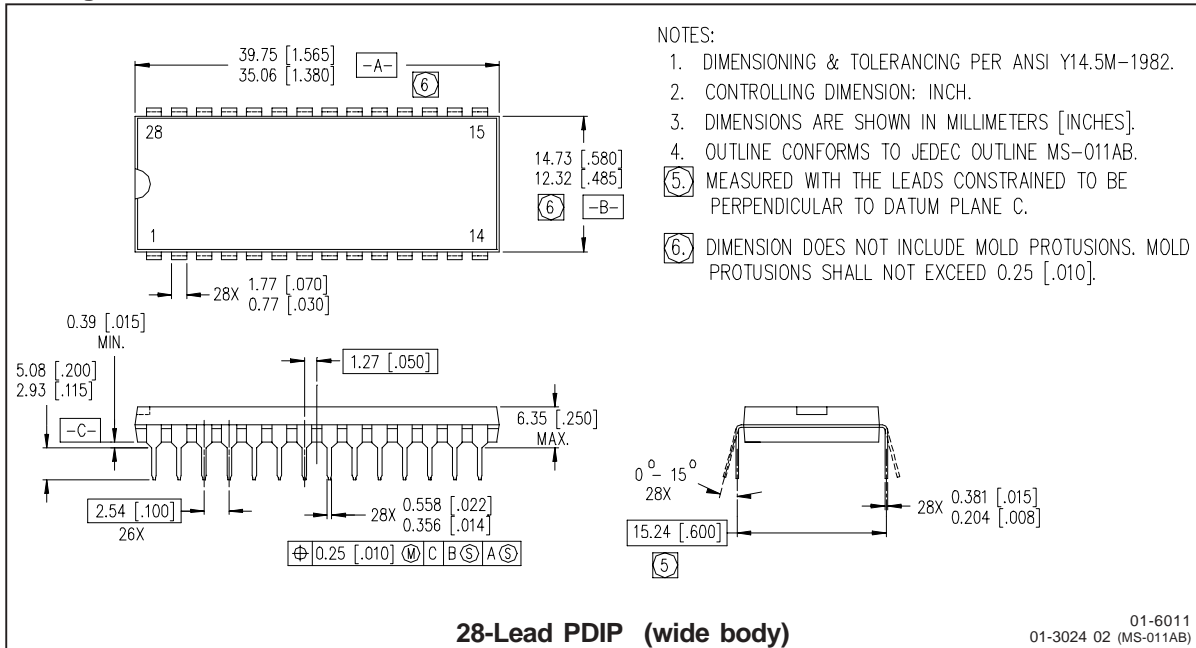
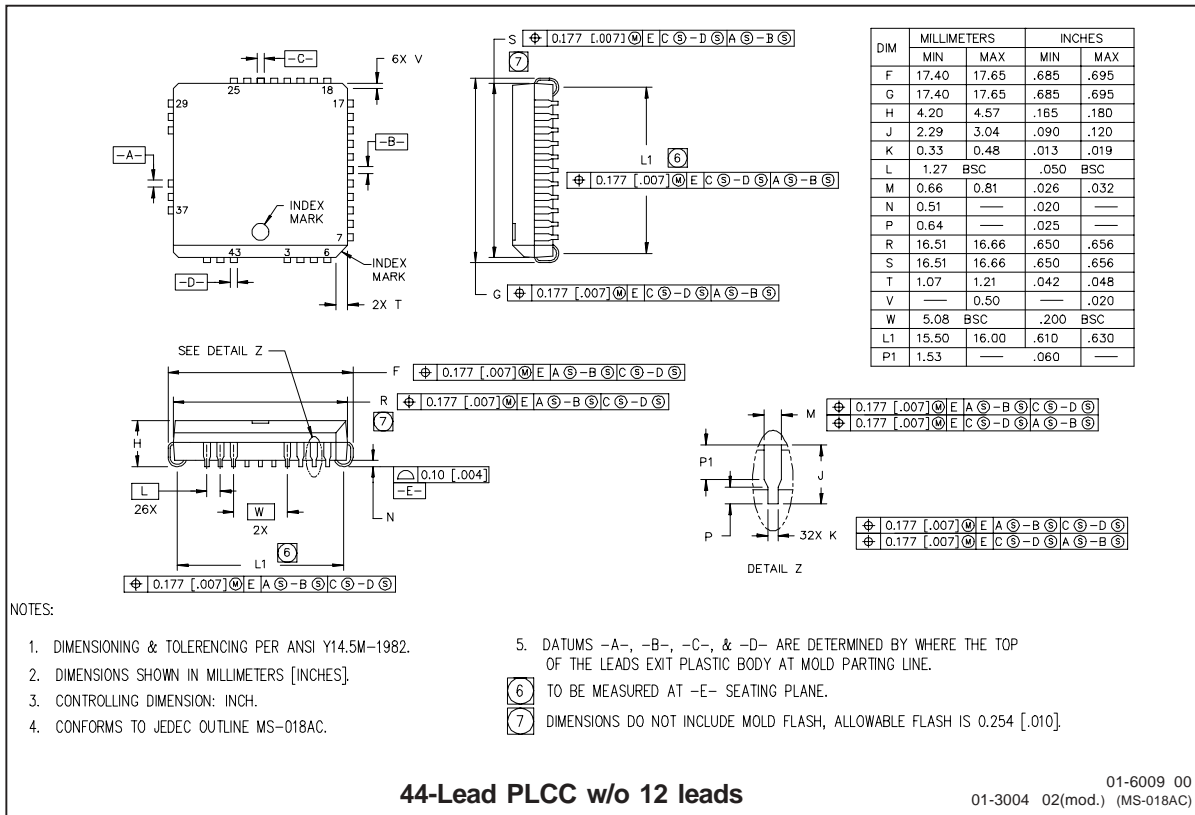
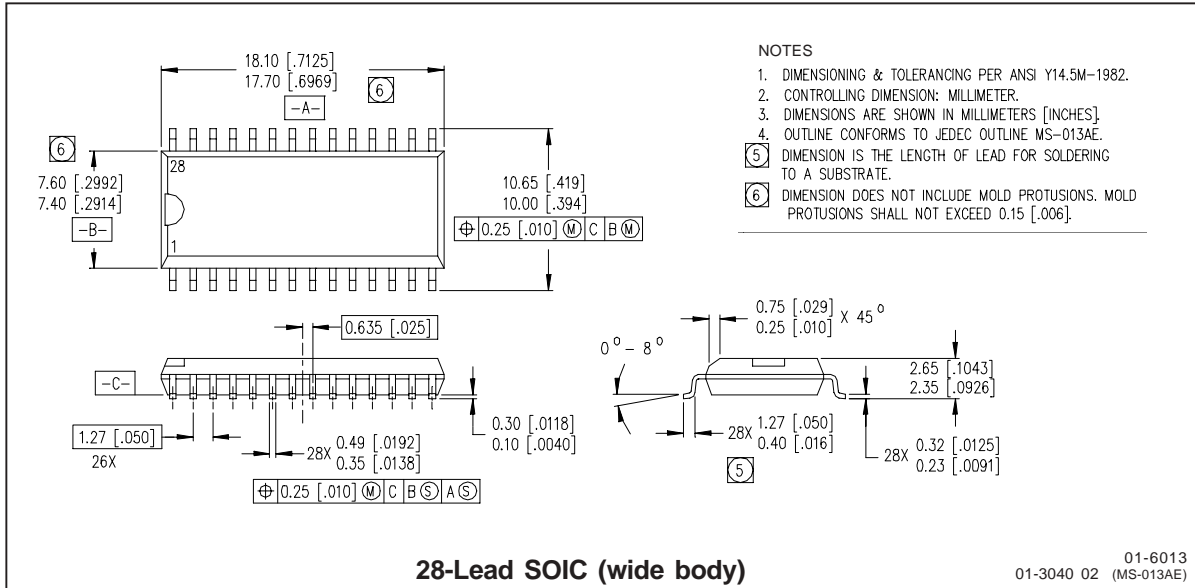


Figure 14. IR2233J Junction Temperature vs Frequency Driving (IRG4ZH71KD) Rgate = 5Ω @ Vcc = 15V

Package Dimensions



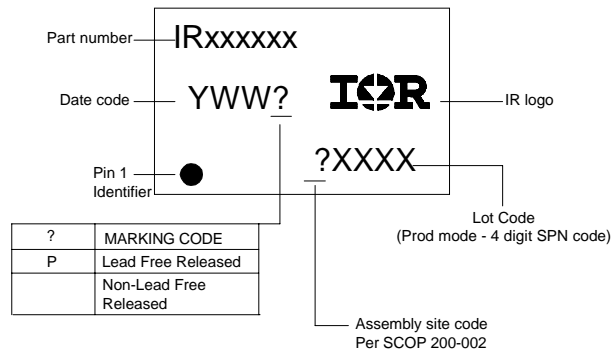
IR2133/IR2135/IR2233/IR2235(J&S) & (PbF)



IR2133/IR2135/IR2233/IR2235(J&S) & (PbF)



LEADFREE PART MARKING INFORMATION



ORDER INFORMATION

Basic Part (Non-Lead Free)

- 28-Lead PDIP IR2133 order IR2133
- 28-Lead SOIC IR2133S order IR2133S
- 28-Lead PDIP IR2135 order IR2135
- 28-Lead SOIC IR2135S order IR2135S
- 28-Lead PDIP IR2233 order IR2233
- 28-Lead SOIC IR2233S order IR2233S
- 28-Lead PDIP IR2235 order IR2235
- 28-Lead SOIC IR2235S order IR2235S
- 44-Lead PLCC IR2133J order IR2133J
- 44-Lead PLCC IR2135J order IR2135J
- 44-Lead PLCC IR2233J order IR2233J
- 44-Lead PLCC IR2235J order IR2235J

Leadfree Part

- 28-Lead PDIP IR2133 order IR2133PbF
- 28-Lead SOIC IR2133S order IR2133SPbF
- 28-Lead PDIP IR2135 order IR2135PbF
- 28-Lead SOIC IR2135S order IR2135SPbF
- 28-Lead PDIP IR2233 Not available at this time
- 28-Lead SOIC IR2233S Not available at this time
- 28-Lead PDIP IR2235 Not available at this time
- 28-Lead SOIC IR2235S Not available at this time
- 44-Lead PLCC IR2133J order IR2133JPbF
- 44-Lead PLCC IR2135J order IR2135JPbF
- 44-Lead PLCC IR2233J Not available at this time
- 44-Lead PLCC IR2235J Not available at this time



IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245 Tel: (310) 252-7105

This product has been qualified per industrial level
 Data and specifications subject to change without notice. 4/12/2004