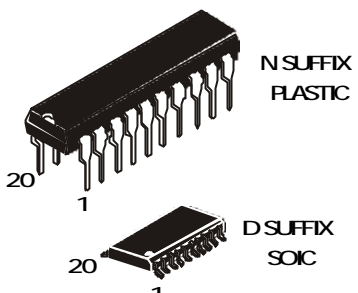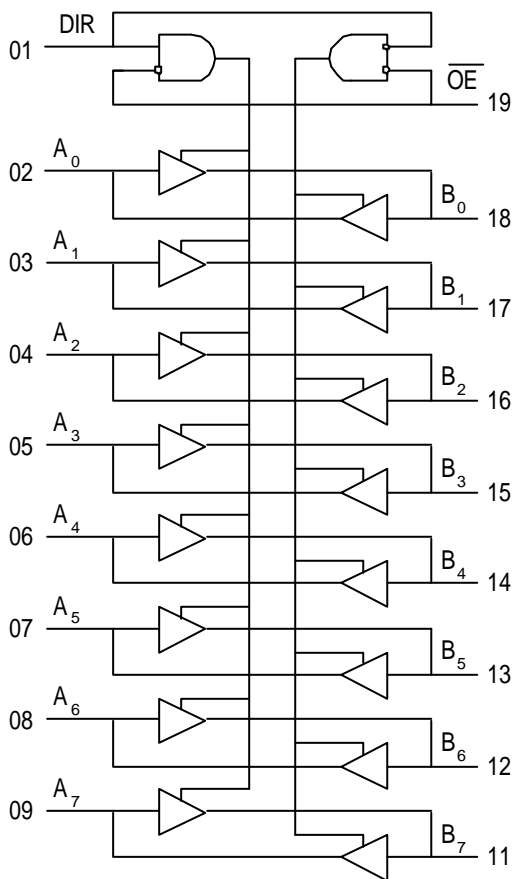# OCTAL BUS TRANSCEIVER (3-State)

By pinning SL74LV245 are compatible with SL74HC245 and SL74HCT245 series. Input voltage levels are compatible with standard CMOS levels.

- Output voltage levels are compatible with input levels of CMOS, NMOS and TTL IC_S
- Supply voltage range: 2.0 to 3.2 V
- Low input current: 1.0 µÀ; 0.1 µÀ at Ò= 25 °Ñ
- Output current 8 mÀ
- Latch current value: not less 150 mÀ at Ò = 125 °Ñ
- ESD acceptable values: not less than 2000 V as per HBM and not less 200 V as per Ì Ì
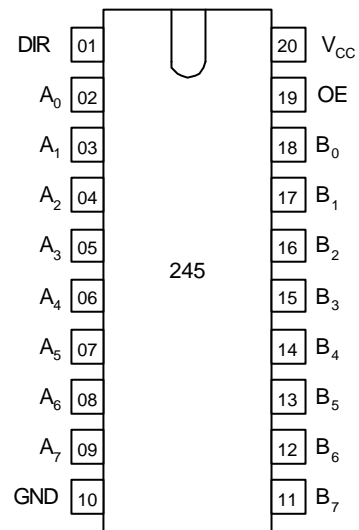-

N SUFFIX
PLASTIC

D SUFFIX
SOIC

ORDERING INFORMATION
SL74LV245N Plastic DIP
SL74LV245D SOIC
T_A = -40° to 125° C
for all packages

BLOCK DIAGRAM

Pin 20=V_{CC}
Pin 10 = GND

PIN ASSIGNMENT

DIR	01	20	V_{CC}
A_0	02	19	OE
A_1	03	18	B_0
A_2	04	17	B_1
A_3	05	16	B_2
A_4	06	15	B_3
A_5	07	14	B_4
A_6	08	13	B_5
A_7	09	12	B_6
GND	10	11	B_7

245

FUNCTION TABLE

Inputs		Inputs/Outputs	
$\overline{OE}$	DIR	À	Â
L	L	A=B	input
L	H	input	B=A
H	X	Z	Z

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Rating	Unit
V_{CC}	Supply voltage	-0.5 to +5.0	V
I_{IK} *1	Input diode current	±20	mÀ
I_{OK} *2	Output diode current	±50	mÀ
I_O *3	Output source or sink current	±35	mÀ
I_{CC}	V_{CC} current	±70	mÀ
I_{GND}	GND current	±70	mÀ
P_D	Power dissipation per package: Plastic DIP *4 SOIC *4	 750 500	mW
Tstg	Storage temperature range	-65 to +150	°C

* In absolute maximum ratings modes functioning is not guaranteed. Vpon lifting the absolute maximum ratings functioning is guaranteed at the recommended operating conditions.
*1 Provided V_I < -0.5 V or V_I > V_{CC} + 0.5 V.
*2 Provided V_O < -0.5 V or V_O > V_{CC} + 0.5 V.
*3 Provided -0.5 V < V_O < V_{CC} + 0.5 V.
*4 When operating in the temperature range of 70°Ñ to 125°C power dissipation value decreases:
- for Plastic DIP by 12 mW/°C
- for SOIC by 8 mW/°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply voltage		1.2	3.6	V
V_{IN}	Input voltage		0	V_{CC}	V
V_{OUT}	Output voltage		0	V_{CC}	V
T_A	Operating ambient temperature range. For all package types		-40	125	°C
t_{LH}, t_{HL}	Input rise and fall times	V_{CC} =1.2 V V_{CC} =2.0 V V_{CC} =3.0 V V_{CC} =3.6 V	0	1000 700 500 400	ns

DC CHARACTERISTICS

Symbol	Parameter	Test conditions	V_{CC}, V	Limits						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
V_{IH}	HIGH level input voltage	$V_O = V_{CC}$-0.1 V	1.2	0.9	-	0.9	-	0.9	-	V
			2.0	1.4	-	1.4	-	1.4	-	
			3.0	2.1	-	2.1	-	2.1	-	
			3.6	2.5	-	2.5	-	2.5	-	
V_{IL}	LOW level output voltage	V_O =0.1 V	1.2	-	0.3	-	0.3	-	0.3	V
			2.0	-	0.6	-	0.6	-	0.6	
			3.0	-	0.9	-	0.9	-	0.9	
			3.6	-	1.1	-	1.1	-	1.1	
V_{OH}	HIGH level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = -50 µÀ	1.2	1.1	-	1.0	-	1.0	-	V
			2.0	1.92	-	1.9	-	1.9	-	
			3.0	2.92	-	2.9	-	2.9	-	
			3.6	3.52	-	3.5	-	3.5	-	
		$V_I = V_{IH}$ or V_{IL} I_O = -8 mÀ	3.0	2.48	-	2.34	-	2.20	-	V
V_{OL}	LOW level output voltage	$V_I = V_{IH}$ or V_{IL} I_O = 50 µÀ	1.2	-	0.09	-	0.1	-	0.1	V
			2.0	-	0.09	-	0.1	-	0.1	
			3.0	-	0.09	-	0.1	-	0.1	
			3.6	-	0.09	-	0.09	-	0.09	
		$V_I = V_{IH}$ or V_{IL} I_O = 8 mÀ	3.0	-	0.33	-	0.4	-	0.5	V
I_I	Input current	$V_I = V_{CC}$ or 0 V	3.6	-	±0.1	-	±1.0	-	±1.0	µÀ
I_{OZ}	OFF-state current	3-state outputs $V_I = V_{IL}$ or V_{IH} V_O =V_{CC} or 0 V	3.6	-	±0.5	-	±5	-	±10	µÀ
I_{CC}	Supply current	V_I =V_{CC} or 0 V I_O = 0 µÀ	3.6	-	8.0	-	80	-	160	µÀ

AC CHARACTERISTICS(C_L=50 pF, t_{LH} = t_{HL} = 6.0 ns)

| Symbol	Parameter	Test conditions	V_{CC}, V	Limits						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
t_{PHL}, t_{PLH} from An to Bn, from Bn to An	Propagation delay	Figure 1	1.2 2.0 3.0	- - -	100 23 14	- - -	125 28 18	- - -	140 34 21	ns
t_{PHZ} t_{PLZ} from OE, DIR to An, Bn	3-state output enable time	Figure 2	1.2 2.0 3.0	- - -	120 30 20	- - -	140 37 24	- - -	160 43 28	ns
t_{PZH} t_{PZL} from OE to An, Bn	3-state output disable time	Figure 2	1.2 2.0 3.0	- - -	120 28 17	- - -	140 35 21	- - -	160 43 26	
t_{THL}, t_{TLH}	HIGH-to-LOW and LOW-to HIGH transition time	Figure 1	1.2 2.0 3.0	- - -	60 15 10	- - -	75 20 13	- - -	90 24 15	
C_I	Input capacitance	For inputs 01,19	3.0	-	7	-	-	-	-	pF
$C_{I/\hat{I}}$	Input capacitance	For inputs/ outputs 02-09, 11-18	3.0	-	20	-	-	-	-	
C_{PD}	Power dissipation capacitance (per one channel)	V_I = 0 V or V_{CC}	3.0	-	50	-	-	-	-	
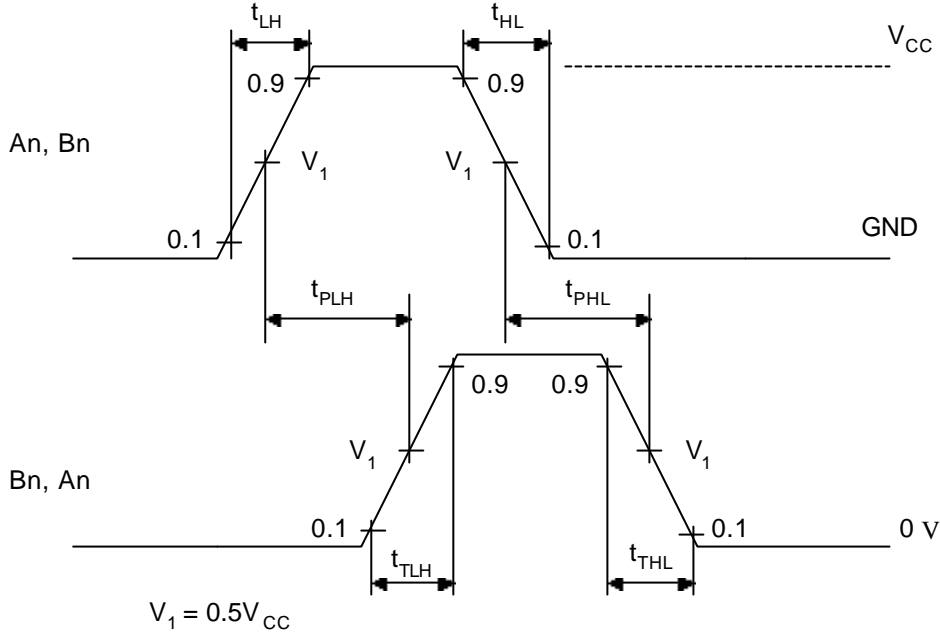
Figure 1 -Time diagram of AC parameters control t_{PLH}, t_{PHL}.
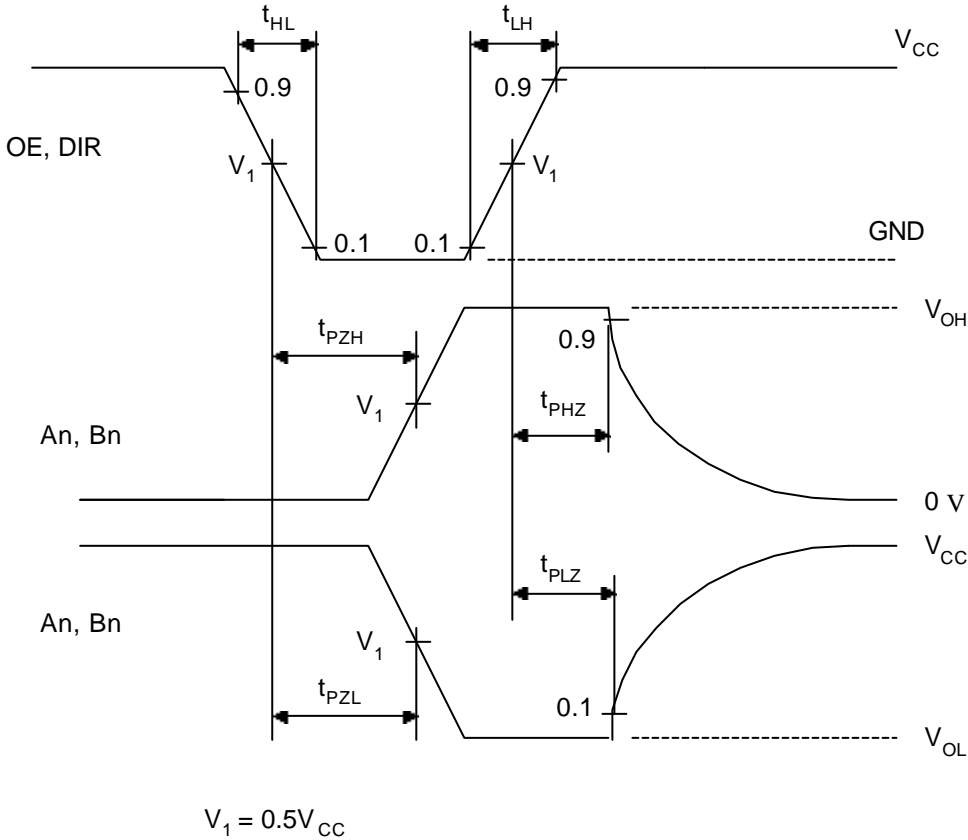
Figure 2 - Time diagram of t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}. AC parameters control

On-chip marking

74LV245
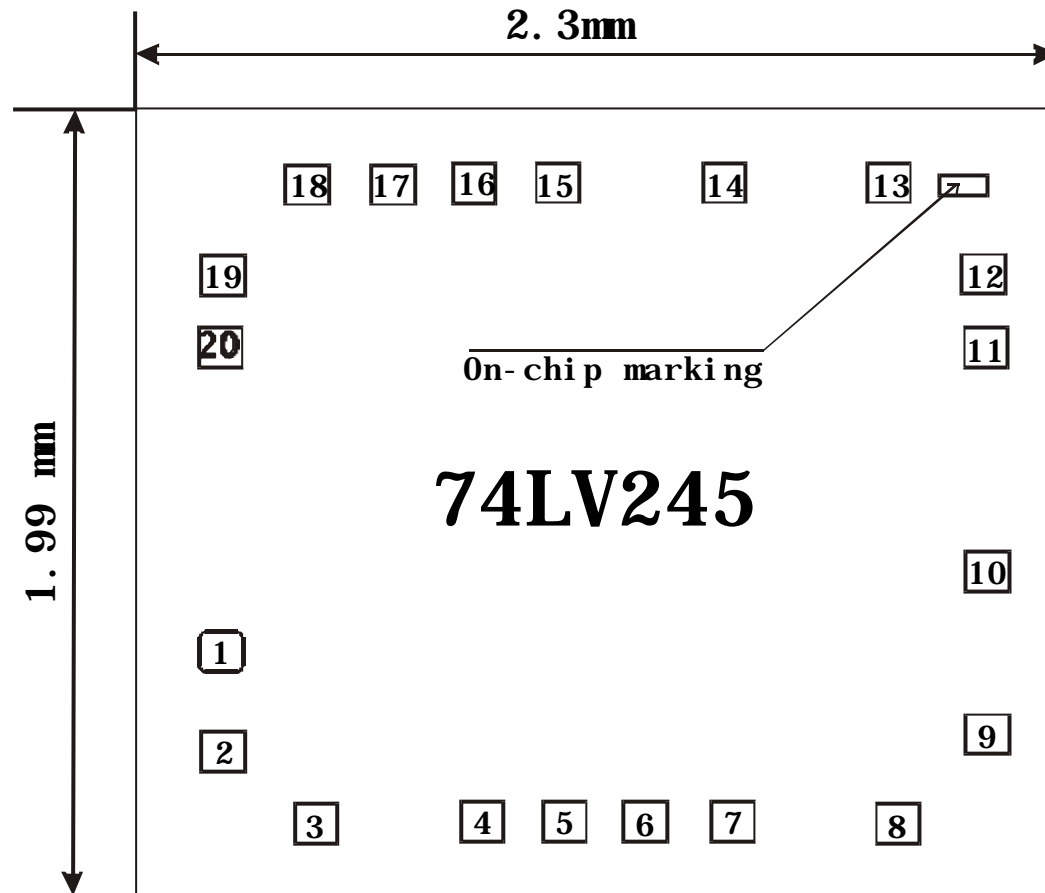
Drawing of the chip

Pads allocation Table

Pad number	coordinates (counted from lower left corner), mm		Pad size, mm
	X	Y	
01	0.140	0.573	0.108 x 0.108
02	0.140	0.315	0.108 x 0.108
03	0.370	0.140	0.108 x 0.108
04	0.790	0.140	0.108 x 0.108
05	1.000	0.140	0.108 x 0.108
06	1.200	0.140	0.108 x 0.108
07	1.417	0.140	0.108 x 0.108
08	1.833	0.140	0.108 x 0.108
09	2.060	0.354	0.108 x 0.108
10	2.060	0.760	0.108 x 0.108
11	2.060	1.340	0.108 x 0.108
12	2.060	1.520	0.108 x 0.108
13	1.833	1.750	0.108 x 0.108
14	1.415	1.750	0.108 x 0.108
15	1.000	1.750	0.108 x 0.108
16	0.790	1.750	0.108 x 0.108
17	0.580	1.750	0.108 x 0.108
18	0.370	1.750	0.108 x 0.108

19	0.140	1.544	0.108 x 0.108
20	0.140	1.375	0.108 x 0.108