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# HD74LVC74

Dual D-type Flip Flops with Preset and Clear

## HITACHI

ADE-205-066C(Z)

Rev.3

September 1995

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### Description

The HD74LVC74 has independent data, preset, clear, and clock inputs Q and  $\bar{Q}$  outputs in a 14 pin package. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input. Low voltage and high speed operation is suitable at the battery drive product (note type personal computer) and low power consumption extends the life of a battery for long time operation.

### Features

- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$
- All inputs  $V_{IH} (\text{Max.}) = 5.5\text{ V} (@V_{CC} = 0\text{ V to }5.5\text{ V})$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V} (@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C})$
- High output current  $\pm 24\text{ mA} (@V_{CC} = 3.0\text{ V to }5.5\text{ V})$

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## Function Table

Inputs				Outputs	
PR	CLR	CK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H <sup>1</sup>	H <sup>1</sup>
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	H	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>
H	H	↓	X	Q <sub>0</sub>	$\bar{Q}$ <sub>0</sub>

H: High level

L: Low level

X: Immaterial

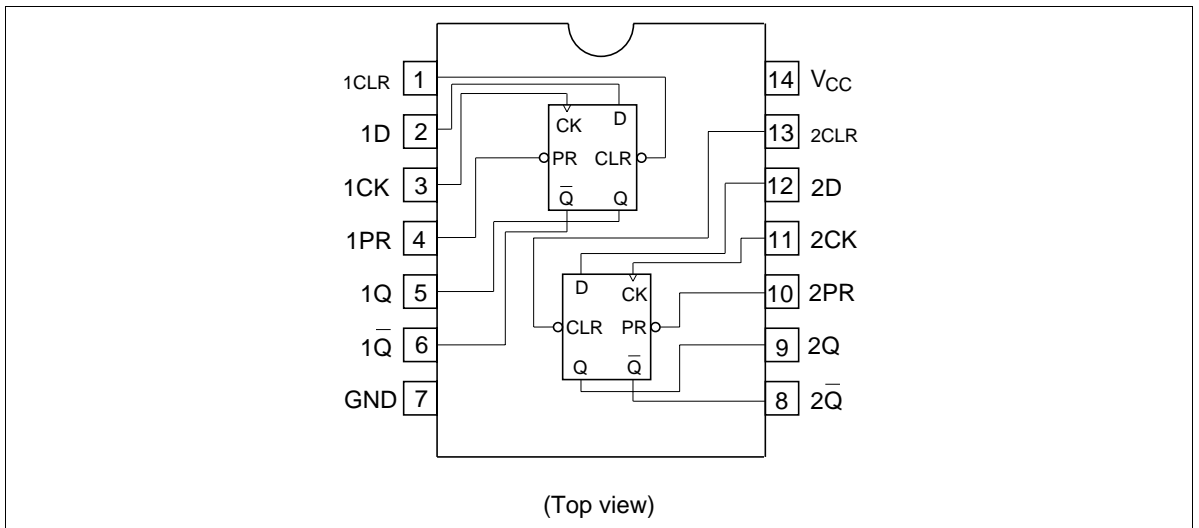
↓: High to Low transition

↑: Low to high transition

Q<sub>0</sub>: Level to Q before the indicated steady input conditions were established.

Note: 1. Q and  $\bar{Q}$  will remain high as long as preset and clear are low, but Q and  $\bar{Q}$  are unpredictable, if preset and clear go high simultaneously.

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 6.0	V	
Input diode current	$I_{IK}$	-50	mA	$V_I = -0.5$ V
Input voltage	$V_I$	-0.5 to 6.0	V	
Output diode current	$I_{OK}$	-50	mA	$V_O = -0.5$ V
		50	mA	$V_O = V_{CC} + 0.5$ V
Output voltage	$V_O$	-0.5 to $V_{CC} + 0.5$ V		
Output current	$I_O$	$\pm 50$	mA	
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	100	mA	
Storage temperature	$T_{stg}$	-65 to +150	°C	

Note: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	1.5 to 5.5	V	Data retention
		2.0 to 5.5	V	At operation
Input / output voltage	$V_I$	0 to 5.5	V	PR, CLR, CK, D
	$V_O$	0 to $V_{CC}$	V	$Q, \bar{Q}$
Operating temperature	$T_a$	-40 to 85	°C	
Output current	$I_{OH}$	-12	mA	$V_{CC} = 2.7$ V
		-24 <sup>*2</sup>	mA	$V_{CC} = 3.0$ V to 5.5 V
	$I_{OL}$	12	mA	$V_{CC} = 2.7$ V
		24 <sup>*2</sup>	mA	$V_{CC} = 3.0$ V to 5.5 V
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	10	ns/V	

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform : Refer to test circuit of switching characteristics.

2. duty cycle  $\leq 50\%$

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## Electrical Characteristics

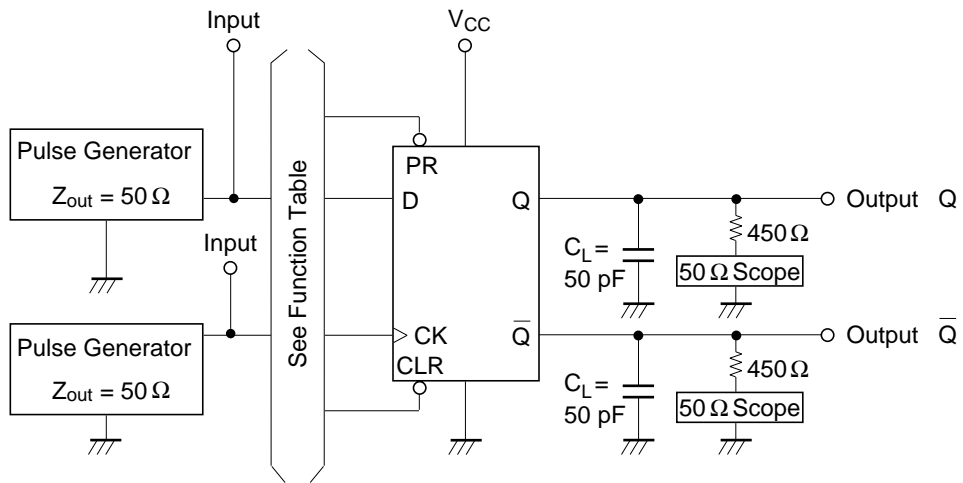
Item	Symbol	$V_{CC}$ (V)	$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions
			Min	Max		
Input voltage	$V_{IH}$	2.7 to 3.6	2.0	—	V	
		4.5 to 5.5	$V_{CC} \times 0.7$	—	V	
	$V_{IL}$	2.7 to 3.6	—	0.8	V	
		4.5 to 5.5	—	$V_{CC} \times 0.3$	V	
Output voltage	$V_{OH}$	2.7 to 5.5	$V_{CC} - 0.2$	—	V	$I_{OH} = -100 \mu\text{A}$
		2.7	2.2	—	V	$I_{OH} = -12 \text{ mA}$
		3.0	2.4	—	V	
		3.0	2.0	—	V	$I_{OH} = -24 \text{ mA}$
		4.5	3.8	—	V	
	$V_{OL}$	2.7 to 5.5	—	0.2	V	$I_{OL} = 100 \mu\text{A}$
		2.7	—	0.4	V	$I_{OL} = 12 \text{ mA}$
		3.0	—	0.55	V	$I_{OL} = 24 \text{ mA}$
		4.5	—	0.55	V	
Input current	$I_{IN}$	0 to 5.5	—	$\pm 5.0$	$\mu\text{A}$	$V_{IN} = 5.5 \text{ V or GND}$
Quiescent supply current	$I_{CC}$	5.5	—	20	$\mu\text{A}$	$V_{IN} = V_{CC} \text{ or GND}$
	$\Delta I_{CC}$	3.0 to 3.6	—	500	$\mu\text{A}$	$V_{IN} = \text{one input at } (V_{CC} - 0.6)\text{V},$ other inputs at $V_{CC} \text{ or GND}$

**Switching Characteristics**

Item	Symbol	V <sub>CC</sub> (V)	Ta = -40 to 85°C			Unit	From (Input)	To (Output)
			Min	Typ	Max			
Maximum clock frequency	f <sub>max</sub>	2.7	150.0	—	—	MHz		
		3.3±0.3	150.0	—	—	MHz		
		5.0±0.5	150.0	—	—	MHz		
Propagation delay time	t <sub>PLH</sub>	2.7	—	6.0	9.0	ns	CLK	Q, $\bar{Q}$
		3.3±0.3	1.5	5.0	8.0	ns		
		5.0±0.5	—	4.0	6.5	ns		
	t <sub>PHL</sub>	2.7	—	6.5	9.0	ns	PR or CLR	Q, $\bar{Q}$
		3.3±0.3	1.5	5.0	8.0	ns		
		5.0±0.5	—	4.0	6.5	ns		
Setup time	t <sub>su</sub>	2.7	4.0	—	—	ns		
		3.3±0.3	3.0	—	—	ns		
		5.0±0.5	3.0	—	—	ns		
Hold time	t <sub>h</sub>	2.7	2.0	—	—	ns		
		3.3±0.3	2.0	—	—	ns		
		5.0±0.5	2.0	—	—	ns		
Pulse width	t <sub>w</sub>	2.7	4.0	—	—	ns	CK	
		3.3±0.3	4.0	—	—	ns		
		5.0±0.5	4.0	—	—	ns		
		2.7	6.0	—	—	ns	PR or CLR	
		3.3±0.3	5.0	—	—	ns		
		5.0±0.5	4.0	—	—	ns		
Recovery time	t <sub>rec</sub>	2.7	3.0	—	—	ns		
		3.3±0.3	2.0	—	—	ns		
		5.0±0.5	2.0	—	—	ns		
Input capacitance	C <sub>IN</sub>	2.7	—	3.0	—	pF		
Output capacitance	C <sub>O</sub>	2.7	—	15.0	—	pF		

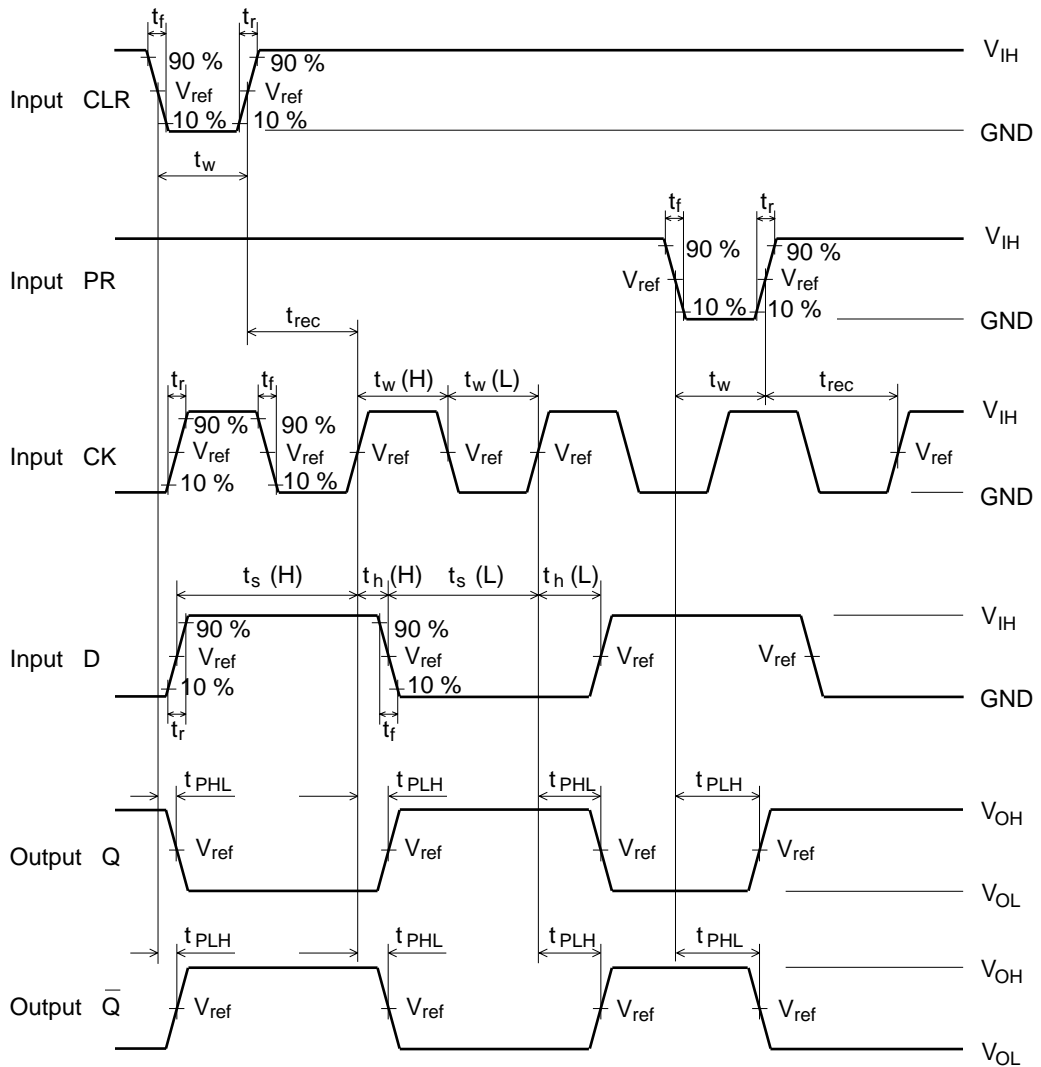
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## Test Circuit



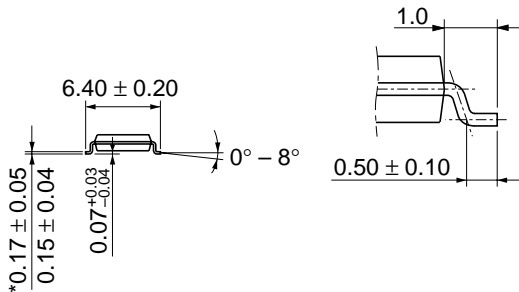
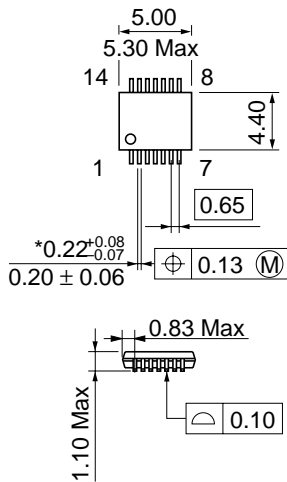
- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2. Test is put into the each flip flops.

## Waveforms



Symbol	$V_{CC} = 2.7 V, 3.3 \pm 0.3 V$	$V_{CC} = 5.0 \pm 0.5 V$
$V_{IH}$	2.7 V	$V_{CC}$
$V_{ref}$	1.5 V	50% $V_{CC}$

- Notes:
- $t_r = 2.5 \text{ ns}$ ,  $t_f = 2.5 \text{ ns}$
  - Clock pulse input waveform : PRR = 10 MHz, duty cycle 50%
  - Data input waveform : PRR = 5 MHz, duty cycle 50%



\*Dimension including the plating thickness  
 Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g



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