

74LVT2245 • 74LVTH2245

Low Voltage Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs and 25Ω Series Resistors in the B Port Outputs

General Description

The LVT2245 and LVTH2245 contain eight non-inverting bidirectional buffers with 3-STATE outputs and are intended for bus-oriented applications. The Transmit/Receive (T/R) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A Ports to B Ports; Receive (active-LOW) enables data from B Ports to A Ports. The Output Enable input, when HIGH, disables both A and B Ports by placing them in a high impedance state. The equivalent 25Ω-series resistor in the B Port helps reduce output overshoot and undershoot.

The LVTH2245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These transceivers are designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT2245 and LVTH2245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Equivalent 25Ω series resistor on B Port outputs
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH2245), also available without bushold feature (74LVT2245)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -12 mA/+12 mA on B Port, -32 mA/+64 mA on A Port
- Latch-up performance exceeds 500 mA

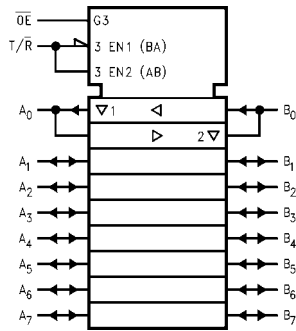
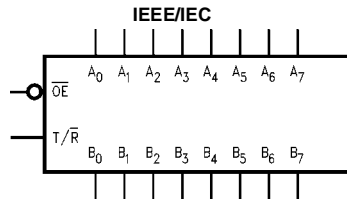
Ordering Code:

Order Number	Package Number	Package Description
74LVT2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVT2245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVT2245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVT2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH2245WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVTH2245SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
74LVTH2245MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVTH2245MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

74LVT2245 • 74LVTH2245 Low Voltage Octal Bidirectional Transceiver with 3-STATE Inputs/Outputs and 25Ω Series Resistors in the B Port Outputs

Logic Symbols



Pin Descriptions

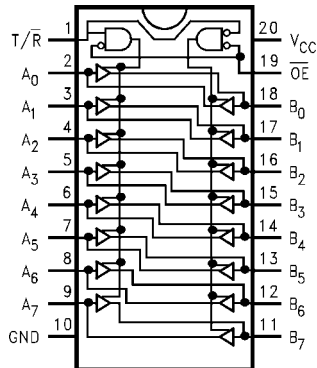
Pin Names	Description
\overline{OE}	Output Enable Input
T/\overline{R}	Transmit/Receive Input
A_0-A_7	Side A Inputs or 3-STATE Outputs
B_0-B_7	Side B Inputs or 3-STATE Outputs

Truth Table

Inputs		Outputs
\overline{OE}	T/\overline{R}	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	HIGH-Z State

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Connection Diagram



Absolute Maximum Ratings (Note 1)				
Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 2)	
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	± 64		mA
I_{GND}	DC Ground Current per Ground Pin	± 128		mA
T_{STG}	Storage Temperature	-65 to +150		$^{\circ}C$
Recommended Operating Conditions				
Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current	A Port	-32	mA
		B Port	-12	
I_{OL}	LOW-Level Output Current	A Port	64	mA
		B Port	12	
T_A	Free Air Operating Temperature	-40	+85	$^{\circ}C$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$, $V_{CC} = 3.0V$	0	10	ns/V
<p>Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.</p> <p>Note 2: I_O Absolute Maximum Rating must be observed.</p>				

DC Electrical Characteristics							
Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions	
			Min	Max			
V _{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	I _I = -18 mA	
V _{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	V _O ≤ 0.1V or	
V _{IL}	Input LOW Voltage	2.7-3.6		0.8	V	V _O ≥ V _{CC} - 0.1V	
V _{OH}	Output HIGH Voltage	A Port	2.7	2.4	V	I _{OH} = -8 mA	
			3.0	2.0		I _{OH} = -32 mA	
		B Port	3.0	2.0	V	I _{OH} = -12 mA	
			2.7-3.6	V _{CC} -0.2	V	I _{OH} = -100 μA	
V _{OL}	Output LOW Voltage	A Port	2.7	0.5	V	I _{OL} = 24 mA	
			3.0	0.4		I _{OL} = 16 mA	
			3.0	0.5		I _{OL} = 32 mA	
			3.0	0.55		I _{OL} = 64 mA	
		B Port	3.0	0.8	V	I _{OL} = 12 mA	
			2.7	0.2	V	I _{OL} = 100 μA	
I _{I(HOLD)} (Note 3)	Bushold Input Minimum Drive	3.0	75		μA	V _I = 0.8V	
I _{I(OD)} (Note 3)	Bushold Input Over-Drive Current to Change State	3.0	500		μA	V _I = 2.0V	
			-500			(Note 4) (Note 5)	
I _I	Input Current	3.6		10	μA	V _I = 5.5V	
			Control Pins	3.6		±1	V _I = 0V or V _{CC}
			Data Pins	3.6		-5	V _I = 0V
						1	V _I = V _{CC}
I _{OFF}	Power Off Leakage Current	0		±100	μA	0V ≤ V _I or V _O ≤ 5.5V	
I _{PU/PD}	Power Up/Down	0-1.5V		±100	μA	V _O = 0.5V to 3.0V	
	3-STATE Current					V _I = GND or V _{CC}	
I _{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.5V	
I _{OZL} (Note 3)	3-STATE Output Leakage Current	3.6		-5	μA	V _O = 0.0V	
I _{OZH}	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.0V	
I _{OZH} (Note 3)	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.6V	
I _{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V	
I _{CCH}	Power Supply Current	3.6		0.19	mA	Outputs High	
I _{CCL}	Power Supply Current	3.6		5	mA	Outputs Low	
I _{CCZ}	Power Supply Current	3.6		0.19	mA	Outputs Disabled	
I _{CCZ+}	Power Supply Current	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled	
ΔI _{CC}	Increase in Power Supply Current (Note 6)	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND	

Note 3: Applies to Bushold versions only (74LVTH2245).

Note 4: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 5: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 6: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 7)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 8)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 8)

Note 7: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 8: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	T _A = -40°C to +85°C C _L = 50 pF, R _L = 500Ω				Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to B Port Output	1.2	4.4	1.2	5.1	ns
t _{PHL}		1.2	4.4	1.2	5.1	
t _{PLH}	Propagation Delay Data to A Port Output	1.2	3.6	1.2	4.0	ns
t _{PHL}		1.2	3.5	1.2	4.0	
t _{PZH}	Output Enable Time for B Port Output	1.3	6.2	1.3	7.3	ns
t _{PZL}		1.7	6.2	1.7	7.3	
t _{PZH}	Output Enable Time for A Port Output	1.3	5.5	1.3	7.1	ns
t _{PZL}		1.7	5.7	1.7	6.7	
t _{PHZ}	Output Disable Time for B Port Output	2.0	5.9	2.0	6.5	ns
t _{PLZ}		2.0	5.4	2.0	5.7	
t _{PHZ}	Output Disable Time for A Port Output	2.0	5.9	2.0	6.5	ns
t _{PLZ}		2.0	5.0	2.0	5.1	
t _{OSSL}	A Port Output to Output Skew (Note 9)		1.0		1.0	ns
t _{OSLH}						
t _{OSSL}	B Port Output to Output Skew (Note 9)		1.0		1.0	ns
t _{OSLH}						

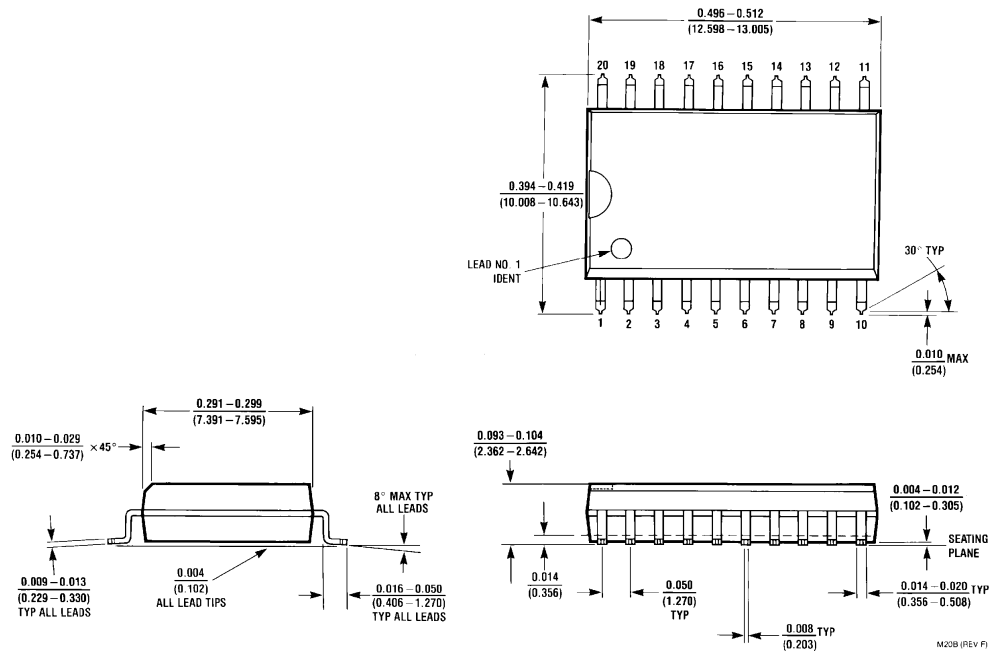
Note 9: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}).

Capacitance (Note 10)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}	4	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

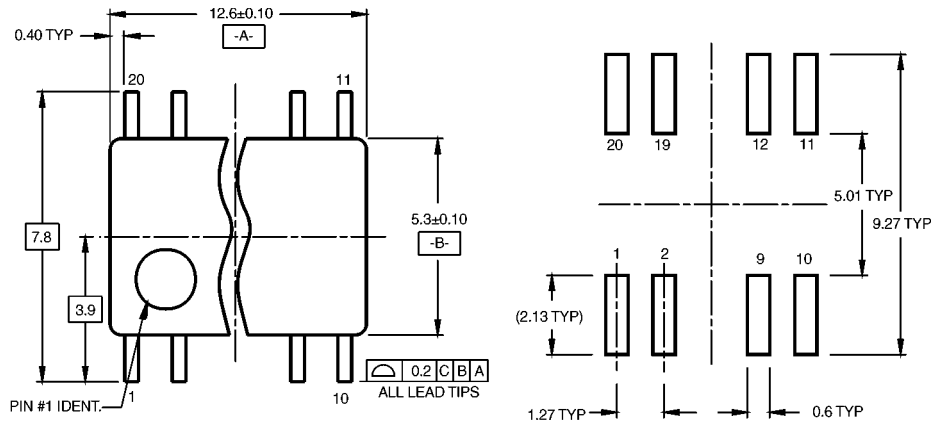
Note 10: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

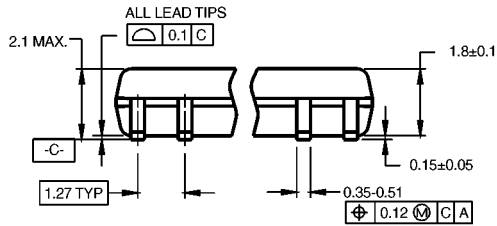


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

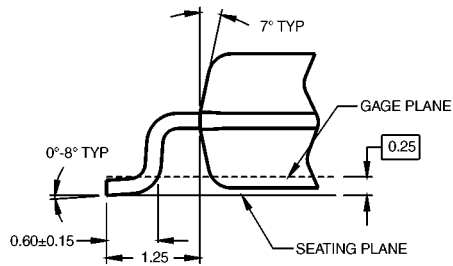
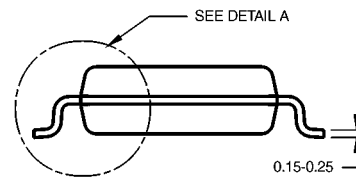
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



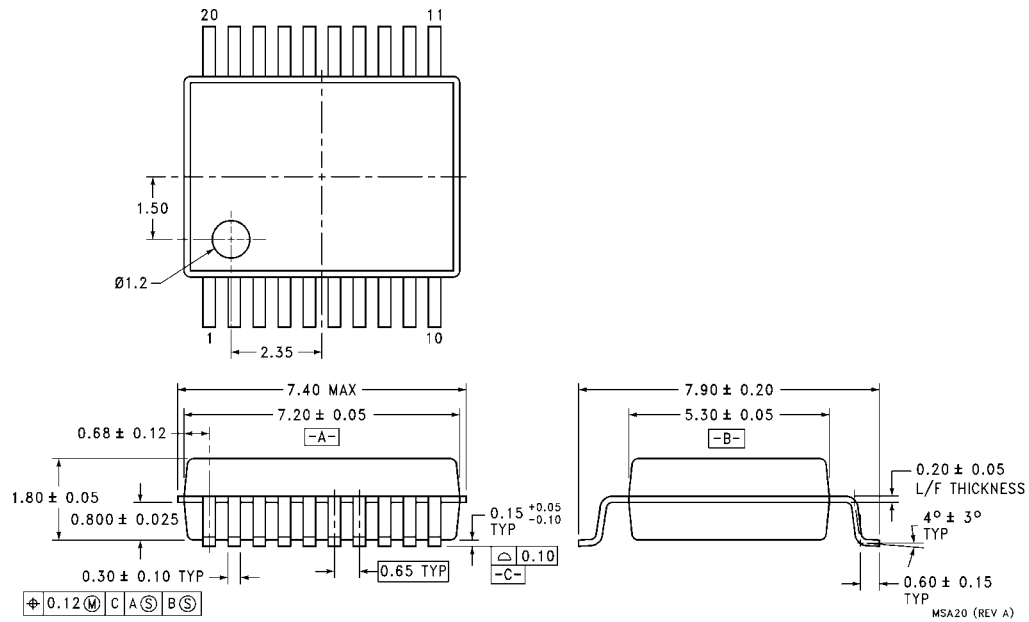
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRvB1

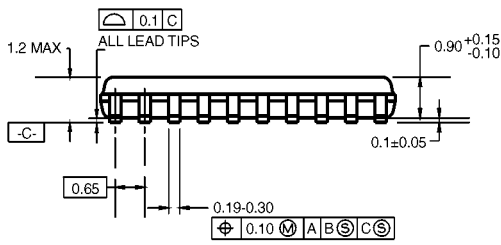
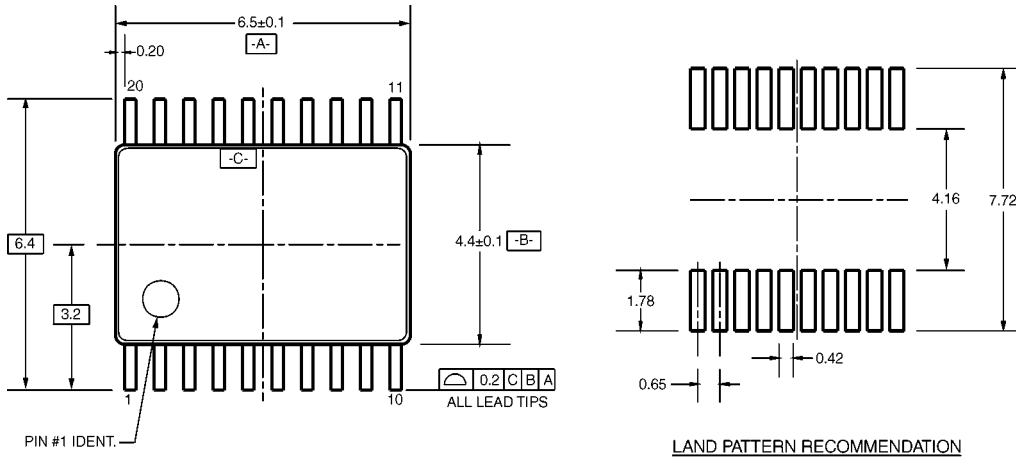
**20-Lead Small Outline Package (SOP), EIAJ TYPE II 5.3mm Wide
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



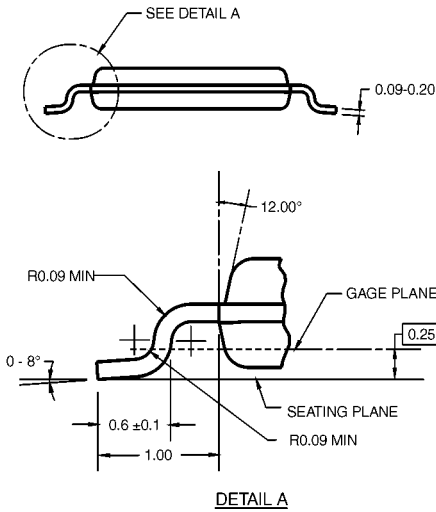
DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com