

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT354

**8-input multiplexer/register with
transparent latches; 3-state**

Product specification
File under Integrated Circuits, IC06

December 1990

8-input multiplexer/register with transparent latches; 3-state

74HC/HCT354

FEATURES

- Transparent data latches
- Transparent address latch
- Easily expanding
- Complementary outputs
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT354 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL

(LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT354 data selectors/multiplexers contain full on-chip binary decoding, to select one-of-eight data sources. The data select address is stored in transparent latches that are enabled by a LOW on the latch enable input (\overline{LE}).

The transparent 8-bit data latches are enabled when the active LOW data enable input (\overline{E}) is LOW. When the output enable input $\overline{OE}_1 = \text{HIGH}$, $\overline{OE}_2 = \text{HIGH}$ or $\overline{OE}_3 = \text{LOW}$, the outputs go to the high impedance OFF-state.

Operation of these output enable inputs does not affect the state of the latches.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	D _n , \overline{E} to Y, \overline{Y}		20	22	ns
	S _n , \overline{LE} to Y, \overline{Y}		24	27	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per latch	notes 1 and 2	68	71	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

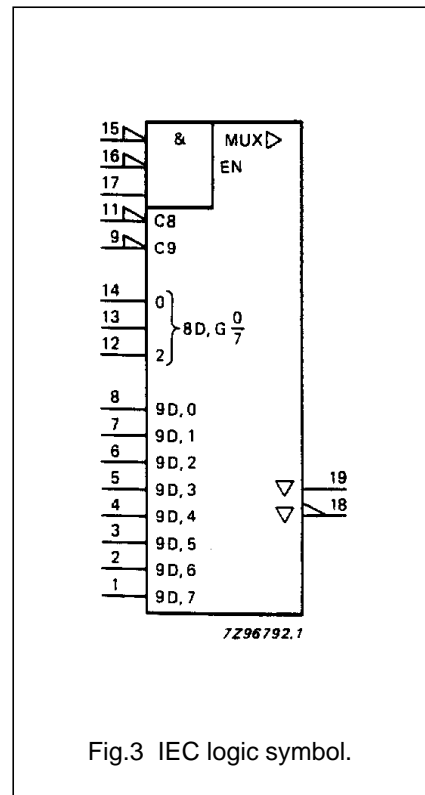
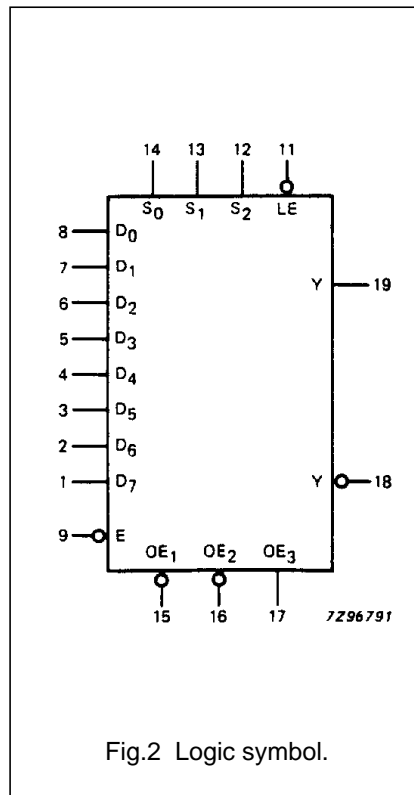
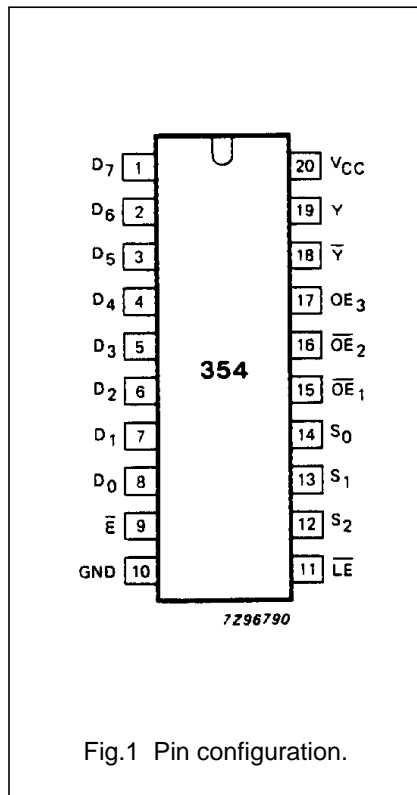
See "74HC/HCT/HCU/HCMOS Logic Package Information".

8-input multiplexer/register with transparent latches; 3-state

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
8, 7, 6, 5, 4, 3, 2, 1	D ₀ to D ₇	data inputs
9	\bar{E}	data enable input (active LOW)
10	GND	ground (0 V)
11	\bar{LE}	address latch enable inputs (active LOW)
14, 13, 12	S ₀ , S ₁ , S ₂	select inputs
15, 16	\overline{OE}_1 , \overline{OE}_2	output enable input (active LOW)
17	OE ₃	output enable input (active HIGH)
18	\bar{Y}	3-state multiplexer output (active LOW)
19	Y	3-state multiplexer output (active HIGH)
20	V _{CC}	positive supply voltage



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FUNCTION TABLE

INPUTS							OUTPUTS		DESCRIPTION
ADDRESS ⁽¹⁾			\overline{E}	OUTPUT ENABLE			Y	\overline{Y}	
S ₂	S ₁	S ₀		\overline{OE}_1	\overline{OE}_2	OE ₃			
X	X	X	X	H	X	X	Z	Z	outputs in high impedance OFF-state
X	X	X	X	X	H	X	Z	Z	
X	X	X	X	X	X	L	Z	Z	
L	L	L	L	L	L	H	D ₀	\overline{D}_0	data latch is transparent
L	L	H	L	L	L	H	D ₁	\overline{D}_1	
L	H	L	L	L	L	H	D ₂	\overline{D}_2	
L	H	H	L	L	L	H	D ₃	\overline{D}_3	
H	L	L	L	L	L	H	D ₄	\overline{D}_4	
H	L	H	L	L	L	H	D ₅	\overline{D}_5	
H	H	L	L	L	L	H	D ₆	\overline{D}_6	
H	H	H	L	L	L	H	D ₇	\overline{D}_7	
L	L	L	H	L	L	H	D _{0n}	\overline{D}_{0n}	data is latched
L	L	H	H	L	L	H	D _{1n}	\overline{D}_{1n}	
L	H	L	H	L	L	H	D _{2n}	\overline{D}_{2n}	
L	H	H	H	L	L	H	D _{3n}	\overline{D}_{3n}	
H	L	L	H	L	L	H	D _{4n}	\overline{D}_{4n}	
H	L	H	H	L	L	H	D _{5n}	\overline{D}_{5n}	
H	H	L	H	L	L	H	D _{6n}	\overline{D}_{6n}	
H	H	H	H	L	L	H	D _{7n}	\overline{D}_{7n}	

Notes

- This column shows the input address set-up with $\overline{LE} = \text{LOW}$ (address latch is transparent).
- D₀ to D₇ = data at inputs D₀ to D₇
D_{0n} to D_{7n} = data at inputs D₀ to D₇ before the most recent LOW-to-HIGH transition of \overline{E}
H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

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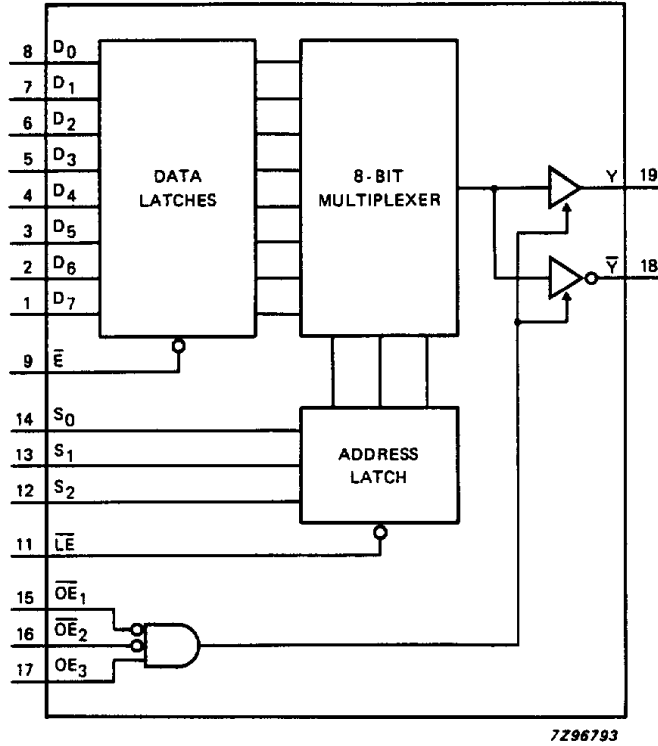


Fig.4 Functional diagram.

8-input multiplexer/register with transparent latches; 3-state

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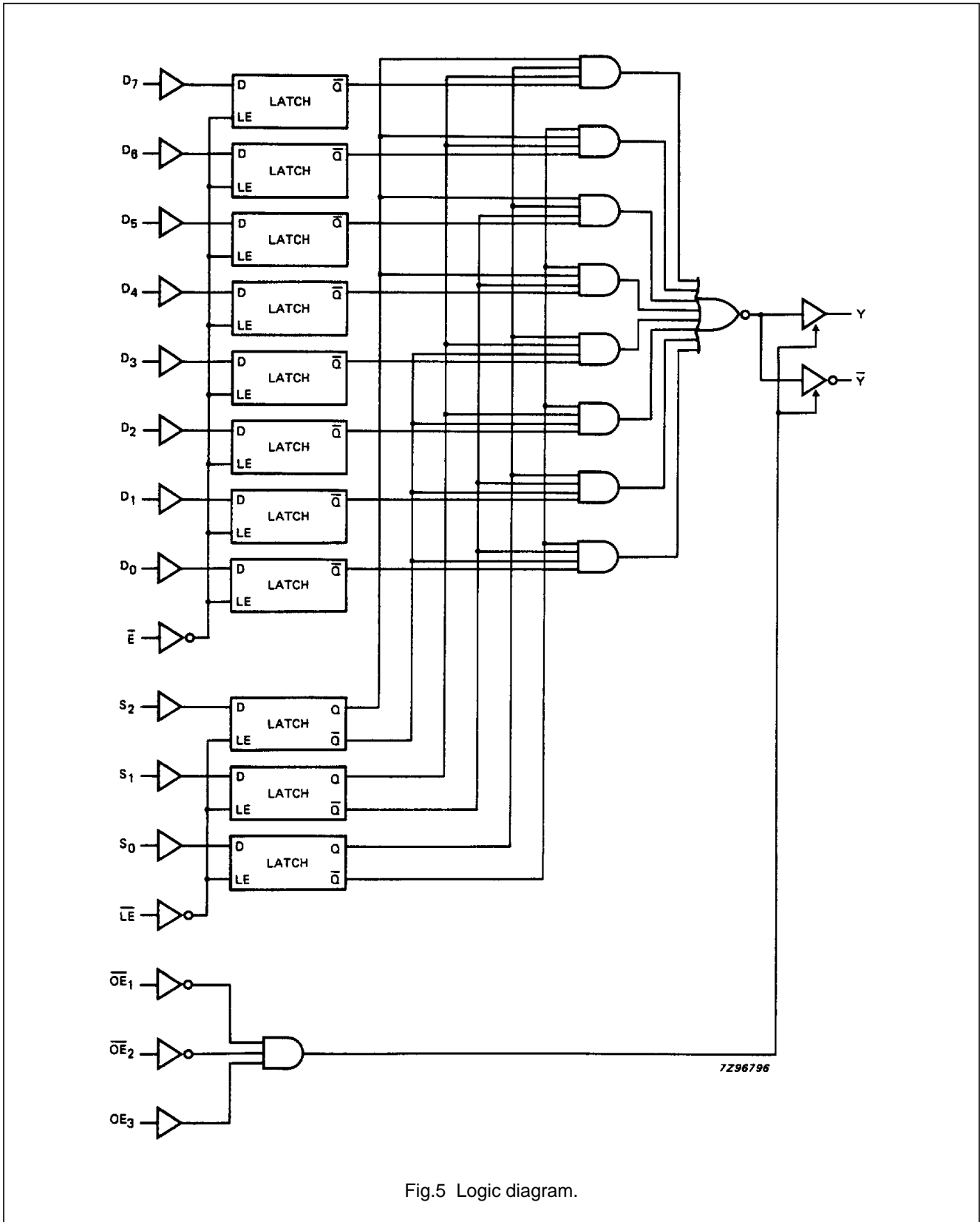


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay D _n to Y, \bar{Y}		61 22 18	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay E to Y, \bar{Y}		63 23 18	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to Y, \bar{Y}		77 28 22	260 52 44		325 65 55		390 78 66	ns	2.0 4.5 6.0	Fig.8
t _{PHL} / t _{PLH}	propagation delay \overline{LE} to Y, \bar{Y}		77 28 22	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig.9
t _{PZH} / t _{PZL}	3-state output enable time OE _n to Y, \bar{Y}		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.10
t _{PZH} / t _{PZL}	3-state output enable time OE ₃ to Y, \bar{Y}		44 16 13	135 27 23		170 34 29		205 41 35	ns	2.0 4.5 6.0	Fig.10
t _{PHZ} / t _{PLZ}	3-state output disable time OE _n to Y, \bar{Y}		50 18 14	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.10
t _{PHZ} / t _{PLZ}	3-state output disable time OE ₃ to Y, \bar{Y}		55 20 16	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig.10
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Figs 7, 8 and 9
t _w	data enable pulse width \bar{E} LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t _w	latch enable pulse width \bar{LE} LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.9

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SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{su}	set-up time D _n to \overline{E}	50	11		65		75		ns	2.0 4.5 6.0	Fig.10
		10	4		13		15				
		9	3		11		13				
t _{su}	set-up time S _n to \overline{LE}	50	14		65		75		ns	2.0 4.5 6.0	Fig.10
		10	5		13		15				
		9	4		11		13				
t _h	hold time D _n to \overline{E}	5	-6		5		5		ns	2.0 4.5 6.0	Fig.11
		5	-2		5		5				
		5	-2		5		5				
t _h	hold time S _n to \overline{LE}	5	-8		5		5		ns	2.0 4.5 6.0	Fig.10
		5	-3		5		5				
		5	-2		5		5				

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74HC/HCT354**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n , S _n	0.2
OE ₃	0.25
\overline{LE}	0.5
\overline{E} , \overline{OE}_n	1.0

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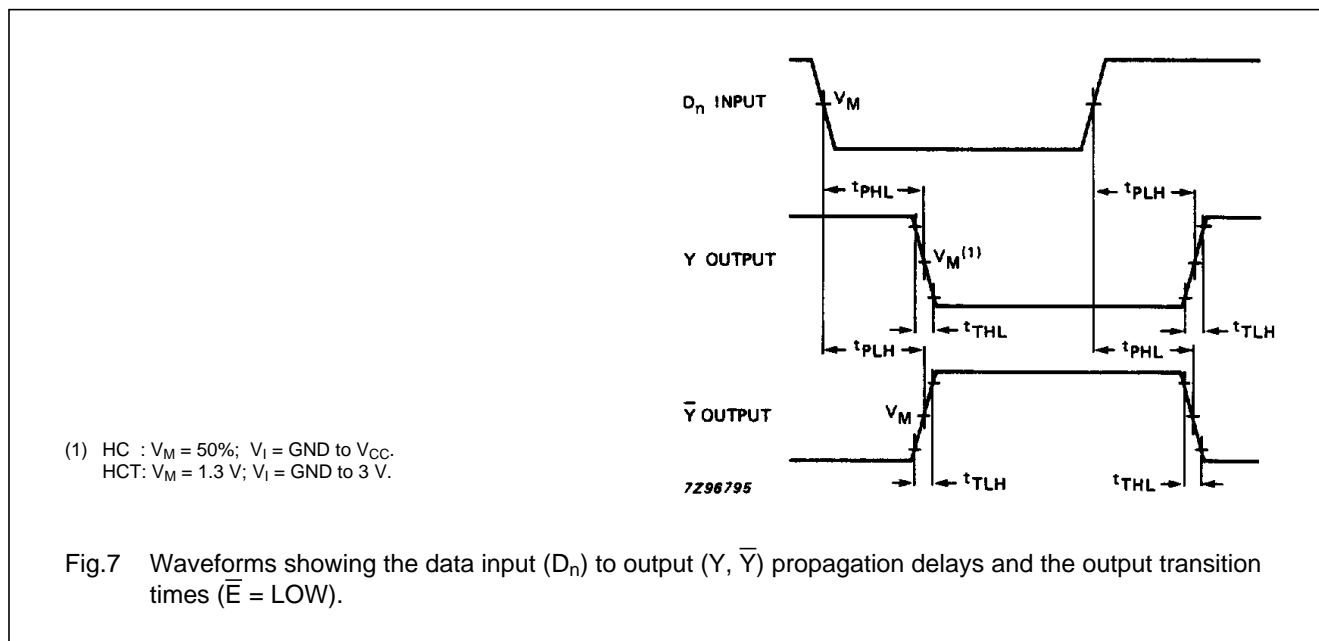
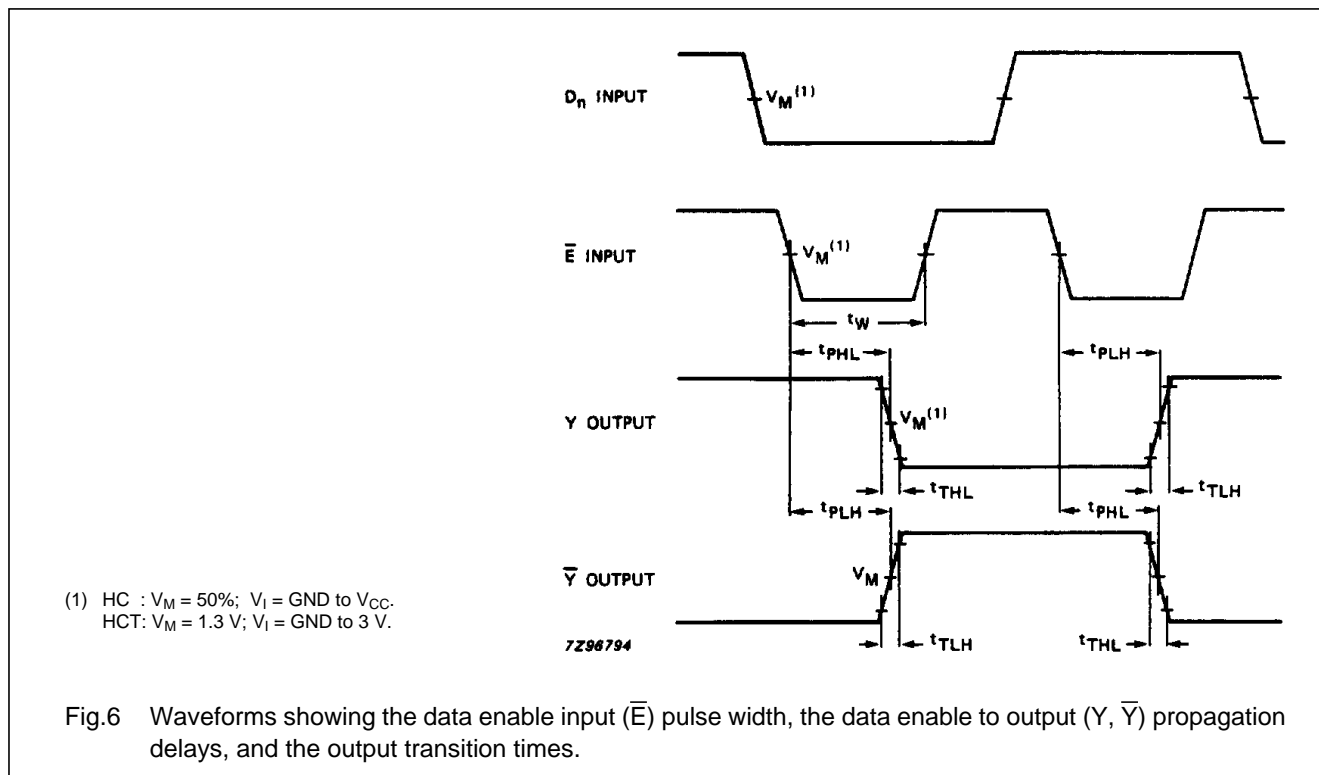
AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V_{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t_{PHL}/t_{PLH}	propagation delay D_n to Y, \bar{Y}		25	47		59		71	ns	4.5	Fig.7	
t_{PHL}/t_{PLH}	propagation delay \bar{E} to Y, \bar{Y}		26	54		68		81	ns	4.5	Fig.6	
t_{PHL}/t_{PLH}	propagation delay S_n to Y, \bar{Y}		30	59		74		89	ns	4.5	Fig.8	
t_{PHL}/t_{PLH}	propagation delay \overline{LE} to Y, \bar{Y}		31	63		79		95	ns	4.5	Fig.9	
t_{PZH}/t_{PZL}	3-state output enable time \overline{OE}_n to Y, \bar{Y}		18	34		43		51	ns	4.5	Fig.10	
t_{PZH}/t_{PZL}	3-state output enable time OE_3 to Y, \bar{Y}		18	34		43		51	ns	4.5	Fig.10	
t_{PHZ}/t_{PLZ}	3-state output disable time \overline{OE}_n to Y, \bar{Y}		18	33		41		50	ns	4.5	Fig.10	
t_{PHZ}/t_{PLZ}	3-state output disable time OE_3 to Y, \bar{Y}		21	39		49		59	ns	4.5	Fig.10	
t_{THL}/t_{TLH}	output transition time		5	12		15		18	ns	4.5	Figs 7, 8 and 9	
t_W	data enable pulse width \bar{E} LOW	16	6		20		24		ns	4.5	Fig.6	
t_W	latch enable pulse width \overline{LE} LOW	16	6		20		24		ns	4.5	Fig.9	
t_{su}	set-up time D_n to \bar{E}	10	4		13		15		ns	4.5	Fig.11	
t_{su}	set-up time S_n to \overline{LE}	10	5		13		15		ns	4.5	Fig.10	
t_h	hold time D_n to \bar{E}	9	0		11		14		ns	4.5	Fig.11	
t_h	hold time S_n to \overline{LE}	9	-3		11		14		ns	4.5	Fig.10	

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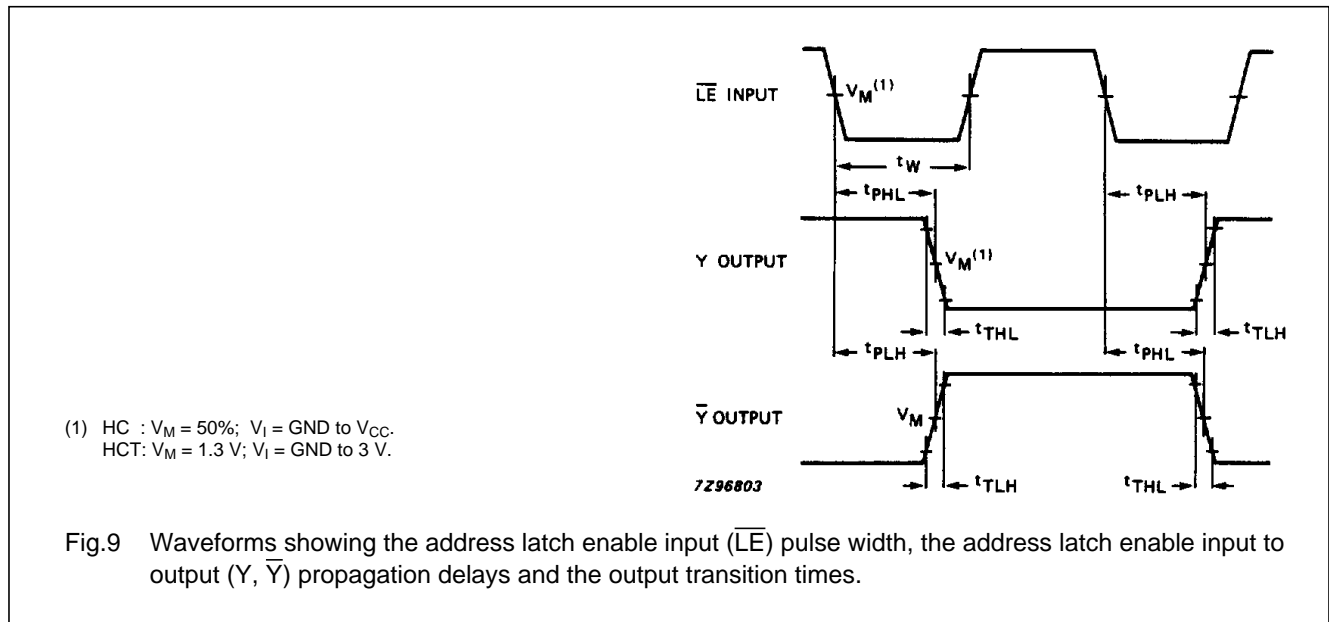
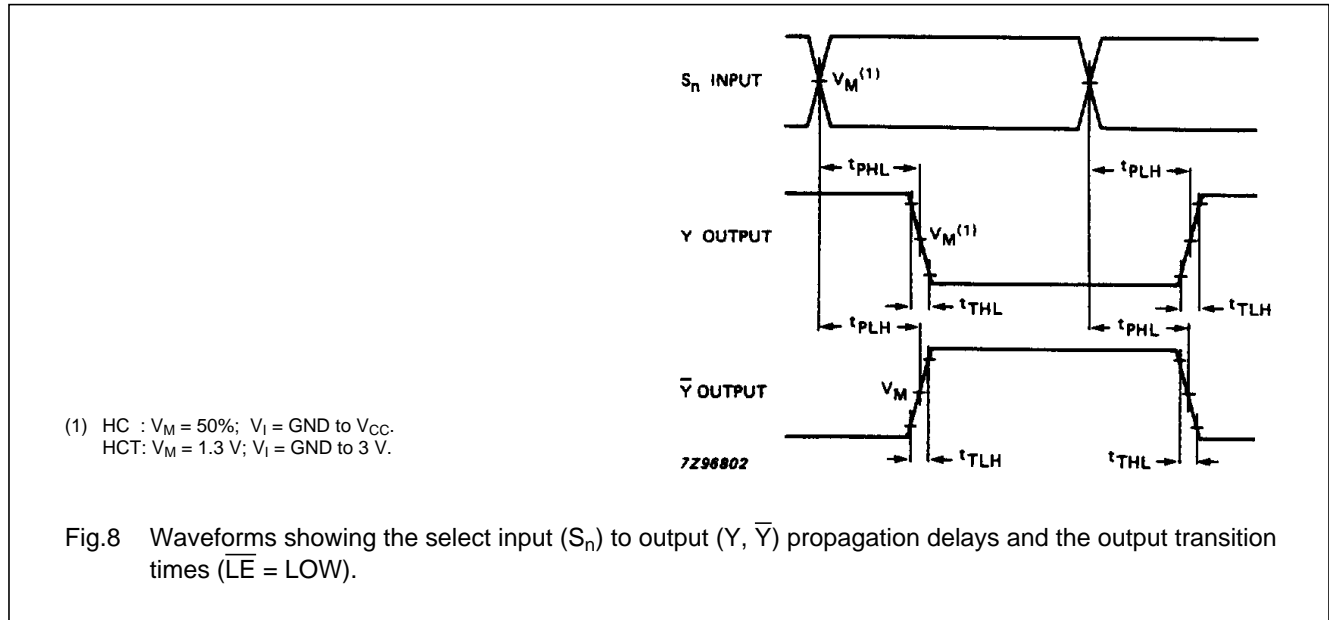
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AC WAVEFORMS



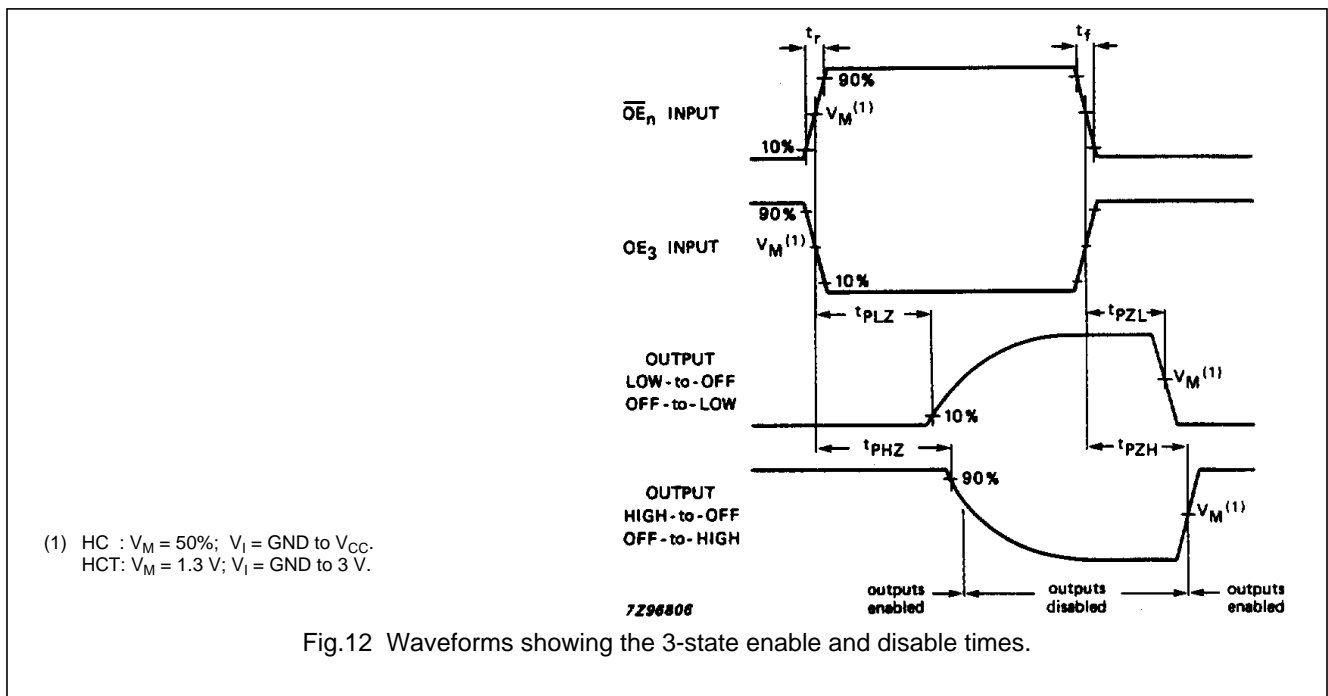
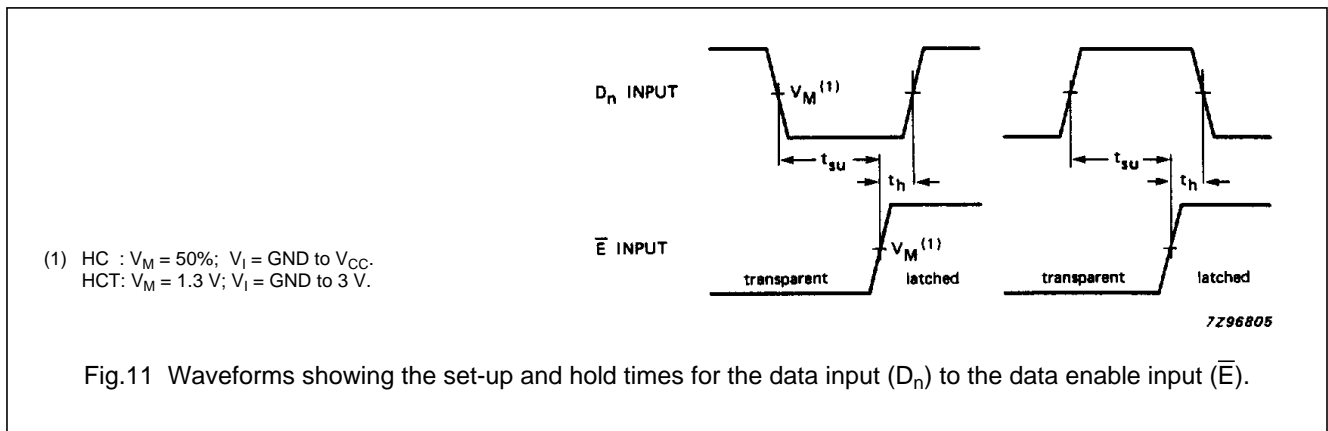
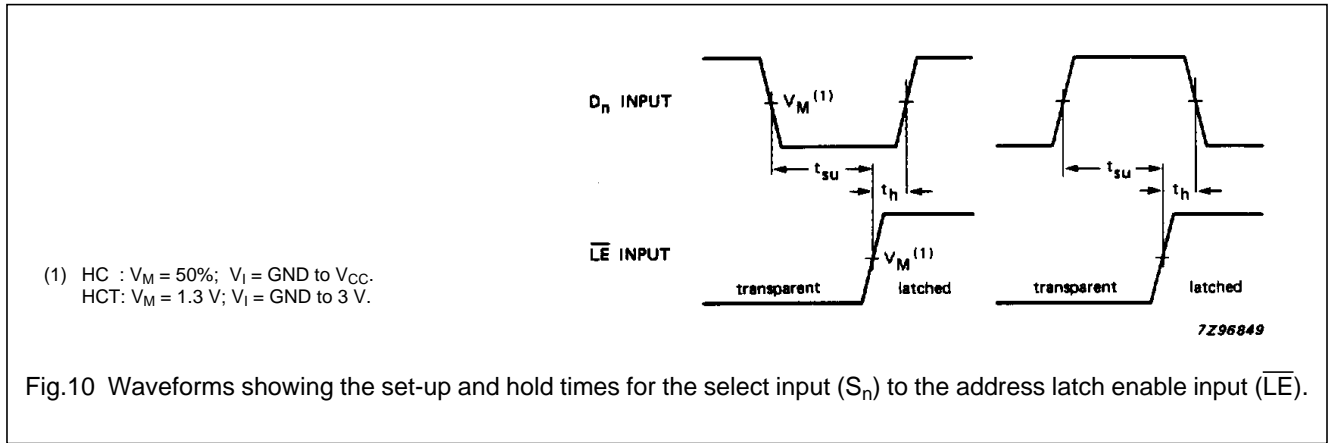
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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.