Digital Subscriber Line Interface Circuit

Preliminary Information

ISSUE 1 August 1993

Features

- Compatible with ISDN U-Interface standard
- Over 40dB (@40 kHz) of loop attenuation
- Full duplex transmission over single twisted pair
- Advanced echo cancelling technology
- High performance 2B1Q line code
- Full activation/deactivation state machine
- QSNR and line attenuation diagnostics
- Frame and superframe synchronization
- On-chip 15 second timer
- Insertion loss measurement test signal & quiet mode
- Mitel ST-BUS compatible
- Single 5V power supply

Applications

- ISDN NT1 and NT2 DSL interface
- Digital PABX line cards and telephone sets
- Digital multiplexers and concentrators
- Pair gain system

Ordering Information

MT8910-1AC 28 Pin Ceramic DIP

MT8910-1AP 44 Pin PLCC

0°C to +70°C

Description

The MT8910-1 Digital Subscriber Line Interface Circuit (DSLIC) is designed to provide ISDN basic rate access (2B+D) at the U-interface. Full duplex digital transmission at 160 kbit/s on a single twisted pair is achieved using echo cancelling hybrid (ECH) technology. This, in conjunction with the high performance 2B1Q line code, allows the DSLIC to meet the loop length requirements of the digital subscriber loops at the U-interface over the entire non-loaded telephone loop plant.

The MT8910-1 is compatible with the complete range of Mitel Semiconductor ISDN components through the use of the ST-BUS interface.

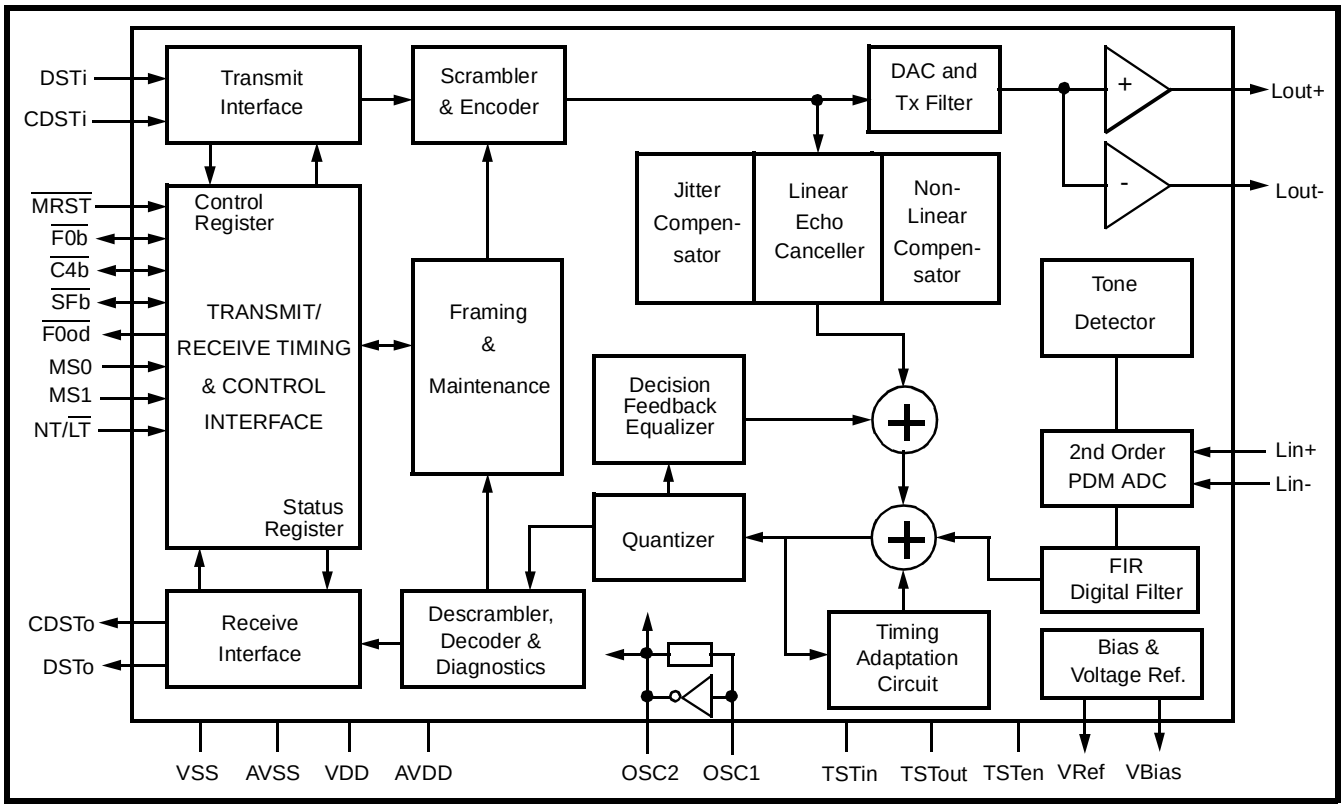


Figure 1 - Functional Block Diagram

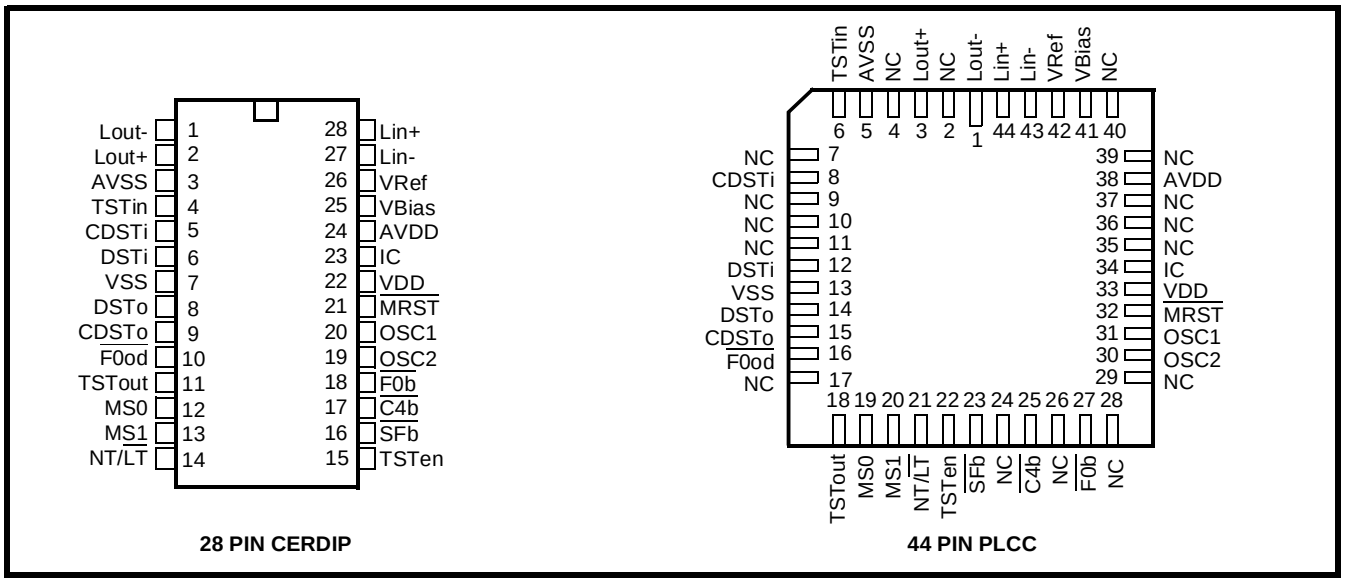


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
DIP	PLCC		
1	1	L_{out-}	**Line Out Minus.** One of a pair of differential analog outputs for the 80 kbaud/s 2B1Q signal, biased at V_{Bias}.
2	3	L_{out+}	**Line Out Plus.** One of a pair of differential analog outputs for the 80 kbaud/s 2B1Q signal, biased at V_{Bias}.
3	5	AV_{SS}	**Analog Ground.** Tie to V_{SS}.
4	6	TSTin	**I/O Structure Test Input.** When TSTen is high, TSTin is used as a source to all output drivers. Refer to “I/O Structure Test" in functional description for more details. Tie to V_{SS} for normal operation.
5	8	CDSTi	**Control/Data ST-BUS Input.** A 2048 kbit/s serial PCM/data input for the D- and C-channels in Dual mode. Unused in Single mode and should be connected to V_{SS}.
6	12	DSTi	**Data ST-BUS Input.** A 2048 kbit/s serial PCM/data input for the D-, C-, B1- and B2-channels in Single mode. In Dual mode, only the B-channels are input.
7	13	V_{SS}	**Ground.**
8	14	DSTo	**Data ST-BUS Output.** A 2048 kbit/s serial PCM/data output for the D-, C-, B1- and B2-channels in Single mode. In Dual mode, only the B-channels are output. This output is placed in high impedance during the unused channel times.
9	15	CDSTo	**Control/Data ST-BUS Output.** A 2048 kbit/s serial PCM/data output for the D- and C- channels in Dual mode. It is placed in high impedance in Single mode, and during the unused channel times in Dual mode.
10	16	$\overline{F0od}$	**Delayed Frame Pulse Output.** A 244 ns wide negative going pulse indicating the end of the active ST-BUS channel times of the device to allow for daisy-chaining of other ST-BUS devices. Active after channel 0 in Dual Port mode and Channel 3 in Single Port Mode.
11	18	TSTout	**I/O Structure Test Output.** When TSTen is high, the TSTout provides the output of an XOR chain which is sourced from all digital inputs. Refer to “I/O Structure Test" in functional description for more details. Leave unconnected for normal operation.
12	19	MS0	**Mode Select 0.** CMOS input. Refer to Table 1.
13	20	MS1	**Mode Select 1.** CMOS input. Refer to Table 1.

Pin Description (continued)

Pin #		Name	Description
DIP	PLCC		
14	21	NT/$\overline{LT}$	**NT/$\overline{LT}$ Mode Select.** CMOS Input. When high, the DSLIC is setup in NT mode. When low, LT mode is selected.
15	22	TSTen	**I/O Structure Test Enable Input.** This active high input enables the built-in test of all digital input and output structures. Refer to “I/O Structure Test" in functional description for more details. Tie to V_{SS} for normal operation.
16	23	$\overline{SFb}$	**Superframe Pulse.** In LT mode, an input pulse once every superframe (12 ms) which, when low during a falling edge of $\overline{C4b}$ within an $\overline{F0b}$ low pulse, sets the transmit superframe boundary. In NT mode, a 244 ns wide output pulse once every 12 ms indicating the boundary of the transmit superframe. In NT mode, the superframe timing is generated from the line signal time base and, as such, $\overline{SFb}$ will only be valid once the transceiver has achieved full activation.
17	25	$\overline{C4b}$	**4096 kHz Data Clock.** In LT mode, a 4096 kHz ST-BUS clock input. In NT mode, a 4096 kHz ST-BUS clock output frequency locked to the line signal.
18	27	$\overline{F0b}$	**Frame Pulse.** In LT mode, an 8 kHz input pulse indicating the start of the active ST-BUS channel times. In NT mode, an 8 kHz output pulse extracted from the line signal indicating the start of the active ST-BUS channel times.
19	30	OSC2	**Oscillator Output.** When the MT8910-1 operates with an External Clock (typically LT mode) connect OSC2 to the output of an external inverter providing a 10.24 MHz ±5ppm clock (see “10.24 MHz Clock Interface" section). When operating with a crystal (typically NT mode) connect one lead of the fundamental mode parallel resonator crystal (10.24 MHz ±50ppm in case of NT mode).
20	31	OSC1	**Oscillator Input.** When the DSLIC operates with an External Clock (typically LT mode) connect OSC1 to the input of an external inverter (see Fig.11). When operating with a crystal (typically NT mode) connect the other lead of the fundamental mode parallel resonator crystal (10.24 MHz ±50ppm in case of NT mode).
21	32	$\overline{MRST}$	**Master Reset.** Active low CMOS input performs a master reset of the DSLIC.
22	33	V_{DD}	**Power Supply Input.**
23	34	IC	**Internal Connection.** Leave unconnected.
24	38	AV_{DD}	**Analog Power Supply.** Connect to V_{DD}.
25	41	V_{Bias}	**Bias Voltage.** Decouple to AV_{SS} through a 1.0 µF ceramic capacitor.
26	42	V_{Ref}	**Reference Voltage.** Decouple to AV_{SS} through a 1.0 µF ceramic capacitor.
27	43	L_{in-}	**Line Signal Input Minus.** Internally biased at V_{Bias}.
28	44	L_{in+}	**Line Signal Input Plus.** Internally biased at V_{Bias}.
	2,4,7, 9 -11, 17,24 26,28 29,35 36,37 39,40	NC	**No Connection.** Leave circuit open.

Functional Description

The MT8910-1 Digital Subscriber Line Interface Circuit (DSLIC) is a high performance, full duplex transceiver which provides a complete interface to the U-reference point as specified in ANSI T1.601-1988. Operating in either master Line Terminator (LT) mode or slave Network Terminator (NT) mode, the DSLIC can be configured to operate at either end of the Digital Subscriber Line (DSL). The DSLIC supports full duplex transmission of a 2B + D-channel format at 160 kbit/s over a single twisted pair with about 40 dB of loop attenuation at 40 kHz. To achieve this transmission performance, the DSLIC uses a 2B1Q line code which is a four level pulse amplitude modulated (PAM) signal with no redundancy. This line code was approved by the American National Standards Institute technical committee T1E1. Using this line code, two binary bits are converted into one four level quaternary symbol. This results in an effective baud rate reduction from 160 to 80 kbaud/s allowing the transmission to benefit from reduced line attenuation and improved immunity to near end crosstalk (NEXT).

To complement the performance of the 2B1Q line code, the DSLIC uses an advanced echo cancelling hybrid (ECH) technique, by means of a transversal filter, that provides greater than 60 dB of echo cancellation. This cancellation, along with all equalization, is performed in the digital domain using dedicated DSP hardware. Since a digital transversal echo canceller gives a linear representation of the echo, the MT8910-1 also has a non-linear echo canceller which works in parallel with the transversal filter to compensate for non-linearities in the transmit path and the passive line termination. In addition, a jitter compensator is used to correct errors in the echo estimates which are sourced from corrections in the received timebase. The jitter compensator will interact directly with the echo taps in the transversal filter.

A block diagram of the DSLIC is shown in Figure 1. The DSLIC has two ports consisting of a serial system interface (Mitel's standard ST-BUS), and a line port which interfaces directly to the single twisted pair via a passive termination hybrid and a line pulse transformer.

The two B-channels and the D-channel to be transmitted on the line are input to the DSLIC (on the ST-BUS) into the transmit interface block. The sync word and maintenance bits are added to the data which is then formatted, scrambled and digitally encoded into 2B1Q symbols. This digital representation is passed through a finite impulse response filter which converts the digital representation into an analog waveform. The transmitted pulse is then passed through a smoothing filter whose output is passed to a differential line driver which is driving the line through a passive hybrid network and line pulse transformer.

On the receive side, the pre-cancelled signal drives a balanced receiver which feeds the input to an over-sampled second-order delta sigma A/D converter. The digital representation of the received signal yields a Pulse Density Modulated (PDM) stream which is digitally filtered and decimated to the 80 kHz baseband. Intersymbol interference (ISI) introduced by the loop is cancelled by a decision feedback equalizer. This is achieved by taking a convolution of the received pulse with the estimated impulse response of the loop. The cancellation of ISI is performed in parallel with the echo cancellation. Estimated received echo is obtained by taking the convolution of the transmit signal with the estimated impulse response of the loop. Feedback from the jitter compensator and the non-linear corrector interact with the coefficients of the echo canceller to reduce the error introduced by jitter and non-linearities in the analog circuitry. The output of all these blocks is summed together and the result is the received data which is passed through a decoder and descrambler before being sent out in TDM bursts on the ST-BUS.

Line Port

The DSLIC interfaces to the U-reference point as defined in the ISDN Basic Access Reference model. As such, the transceiver transfers full duplex, time division multiplexed data at 160 kbit/s. This includes two 64 kbit/s PCM voice or data channels (B-channels), a 16 kbit/s signalling channel (D-channel) and 16 kbit/s for synchronization and overhead.

The two 64 kbit/s channels are defined as the B1- and B2-channels and they carry subscriber information such as digitally encoded voice, circuit switched data or packet switched data. The DSLIC will transfer both B-channels transparently from the ST-BUS port to the line port and vice versa once the device has acquired superframe synchronization.

The 16 kbit/s D-channel is primarily intended to carry signalling information for circuit switching the B-channels through the ISDN network. The D-channel can optionally carry packetized information and telemetry services. The D-channel is transmitted transparently through the DSLIC from the ST-BUS port to the line port and vice versa once the device has acquired superframe synchronization. It is to be

noted that the system interface has dedicated a full 64 kbit/s for the D-channel of which only the two first bits (D0 and D1) are actually carrying information. The other bits of the ST-BUS D-channel are reserved for future use.

A third type of channel, the C-channel, is a non-bearer channel which provides a means for the system to control and monitor the functionality of the DSLIC. This control/status channel is accessed by the system through the ST-BUS. The C-channel provides access to three control registers and four status registers which provide complete control or status of all built-in features. Access to the control register is provided by two bits in the Control Register itself (CRS0 and CRS1). Selection of the desired status register is performed using two bits in Control Register 1 (SRS0 and SRS1). The C-channel also carries a control and status register for the 4 kbit/s M-channel which can be used as an additional maintenance channel. A detailed description of these registers is discussed in the ST-BUS port interface section.

Line Code

The DSLIC transceiver uses the 2B1Q line code which is a four level Pulse Amplitude Modulated (PAM) code with no redundancy. The generation of the 2B1Q signal is achieved by grouping two consecutive bits into a bit field of which the first bit represents the sign bit and the second represents the magnitude. This yields four possible output codes as shown in Figure 3 (note that +3, +1, -1 and -3 are only symbols and they do not reflect the voltage on the line).

The bit fields are grouped relative to the borders of the defined channels where the first bit field consists of bit 1 and bit 2 of the B1-channel, the second bit field consists of bit 3 and bit 4 of the B1-channel and so on.

Before converting the bit fields into output symbols, all bits except the framing pattern are scrambled with polynomials:

$$1 \oplus x^{-5} \oplus x^{-23} \text{ for LT}$$
$$1 \oplus x^{-18} \oplus x^{-23} \text{ for NT}$$

(where $\oplus$ is modulo two summation)

Framing

The frame structure in the DSLIC is 1.5 ms long and consists of twelve 2B+D-channels delimited by the framing pattern at the start of the frame and the maintenance channel at the end. Framing for both the LT and the NT is performed using a 9 symbol synchronization word. This sync word (SW) has the following structure:

Sync Word: +3, +3, -3, -3, -3, +3, -3, +3, +3

Eight DSLIC frames are grouped into a superframe delimited by inverting the sync word (ISW):-3,-3, +3, +3, +3, -3, +3, -3, -3. This second level of framing is used to assign the M-channel bits as defined in the ANSI T1.601-1988. The framing structure is shown in Figure 4.

Transmission between the LT and NT is fully synchronous. As such, the frame/superframe boundaries between the NT receive frame and the NT transmit frame have a fixed phase relationship. The transmitted frame/superframe from the NT is delayed by 60 ± 2 quaternary symbols (quats) with respect to its received frame/superframe. Since the NT extracts all its timing from the line, the DSLIC will maintain the required phase relationship between the frames and superframes and will insert the SW and ISW during the proper time interval.

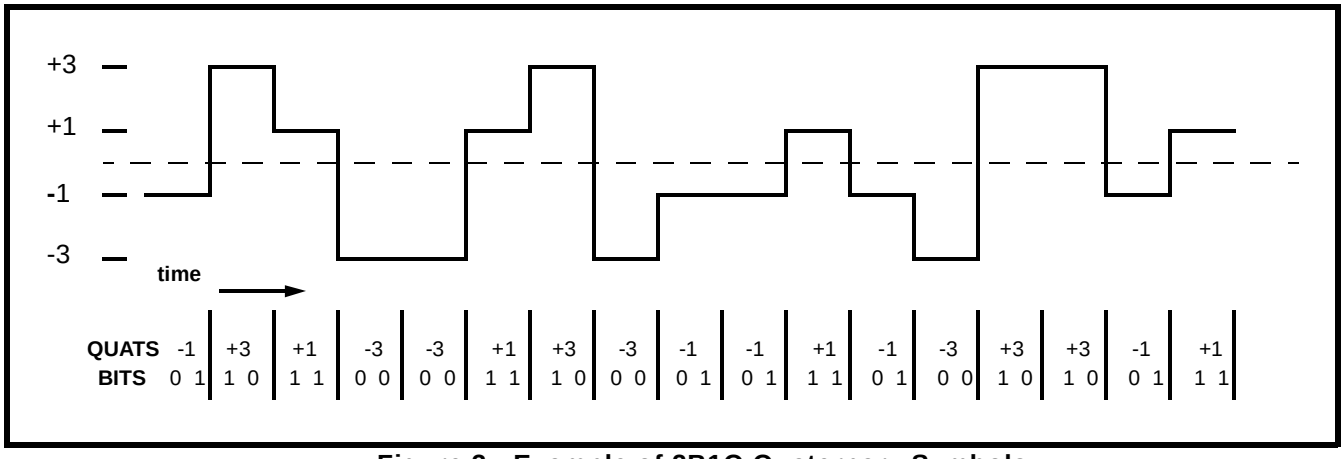


Figure 3 - Example of 2B1Q Quaternary Symbols

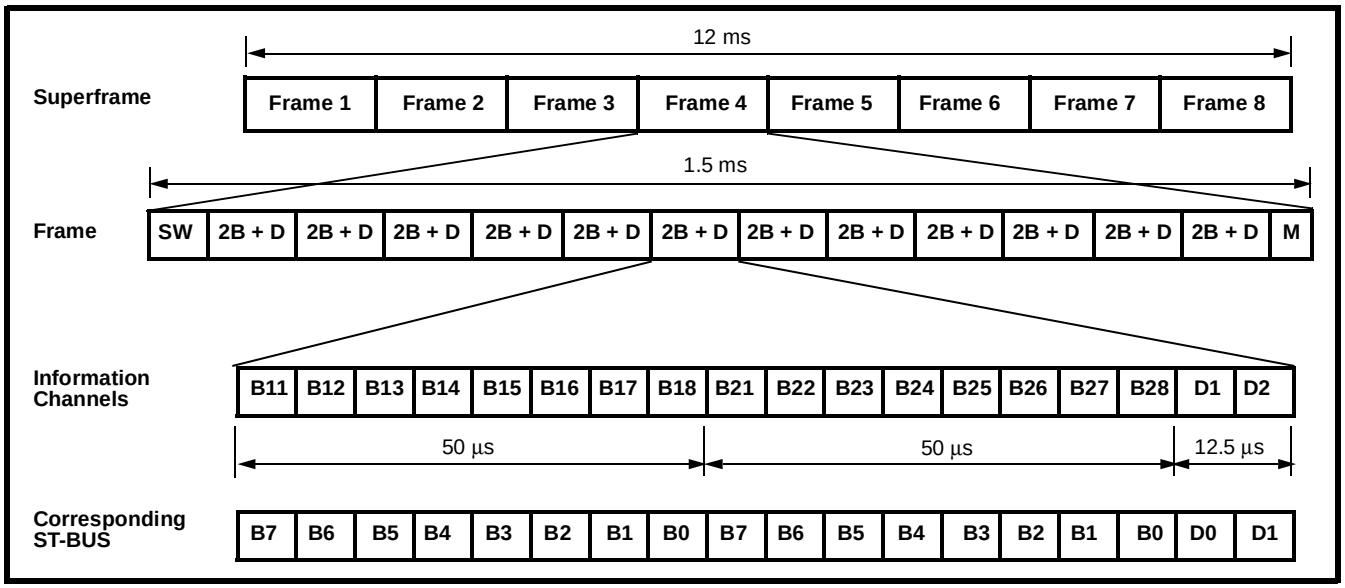


Figure 4 - Frame Structure

Basic Frame Synchronization (BFS) is achieved using the algorithm shown in Figure 5. The DSLIC searches for the sync word or the inverted sync word within the received data stream. After detecting three consecutive synchronization patterns spaced exactly 120 quats apart, the DSLIC declares terminal synchronization by setting the bits of the Internal State Indicator to 111 in Status Register 1. A loss of synchronization is declared by the DSLIC when at least one of the nine quats at the beginning of each Basic Frame differs by more than one quantization level for two consecutive frames.

A search for superframe synchronization will begin only after Basic Frame sync has been found. The DSLIC will declare superframe sync (SFS) on the first occurrence of the properly spaced Inverted Sync Word (ISW) once Basic Frame sync has been acquired. The synchronized state is identified by the status of internal state bits IS2, IS1 and IS0 found in Status Register 1.

The DSLIC will lose superframe sync under three conditions;

1) if the DSLIC loses basic frame sync,

2) if the ISW does not occur exactly eight basic frames apart,

3) if the ISW is received when it is not expected.

Activation/Deactivation

The DSLIC has a complete activation/deactivation state machine which allows the user to activate or deactivate the link as per the requirements in the

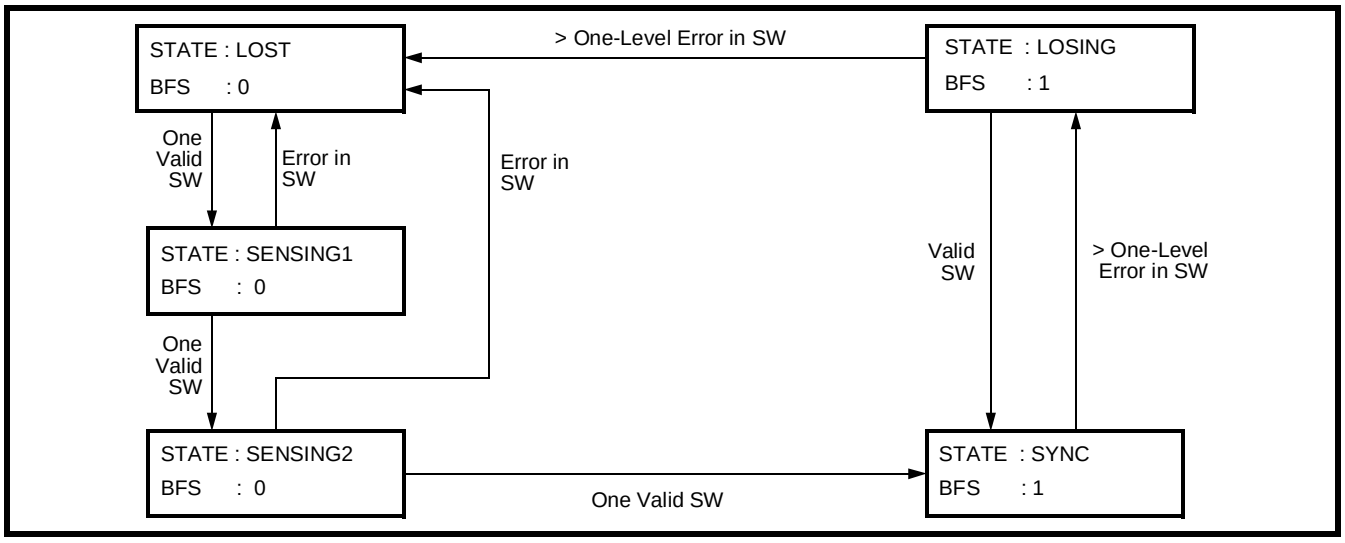


Figure 5 - Frame Synchronization State Diagram

T1.601-1988 standards. The activation sequence for the DSLIC is mode dependent and is outlined in Figures 6a) and b).

In the LT mode, the request for activation can be initiated in two ways. Setting the start/stop bit in the Control Register 1 will result in the generation of a repeated pattern of four +3 symbols followed by four -3 symbols producing a 10 kHz activation tone (TL) for 3 milliseconds. The DSLIC can also be activated by receiving a 10 kHz activation tone from the NT (TN). Once the NT has generated a tone, progression through the state machine follows the algorithm as shown in Figure 6a.

In the NT mode, the request for activation can be initiated in two ways. Setting the start/stop bit in the Control Register 1 will result in the generation of a repeated pattern of four +3 symbols followed by four -3 symbols resulting in the transmission of the NT activation tone (TN). The DSLIC can also be activated by receiving TL from the LT to which the NT will respond with its own activation tone (TN). Progression through the state machine will follow the algorithm as shown in Figure 6b.

During the activation sequence, there is an extensive exchange of signals between the LT and the NT. This handshaking of information is required to allow individual transceivers to train both their echo cancellers and decision feedback equalizers. All possible signals are described below.

- TN: A 10 kHz activation tone sourced by the NT which is generated by sending a continuous pattern of four +3 symbols followed by four -3 symbols.
- SN0: SN0 is a no signal condition which is used to indicate to the LT that the NT has finished training its echo canceller.
- SN1: An NT generated signal consisting of a framed (but not superframed), scrambled 2B1Q signal which carries all 1s in the B-, D- and M-channels. This signal is used to train the NT's echo canceller.
- SN2: An NT generated signal consisting of a framed (but not superframed), scrambled 2B1Q signal which carries all 1s in the B-, D- and M-channels. This signal is used to train the LT's DFE.
- SN3: An NT generated signal consisting of a fully framed and superframed scrambled 2B1Q signal which carries information in all the B-, D- and M-channels.

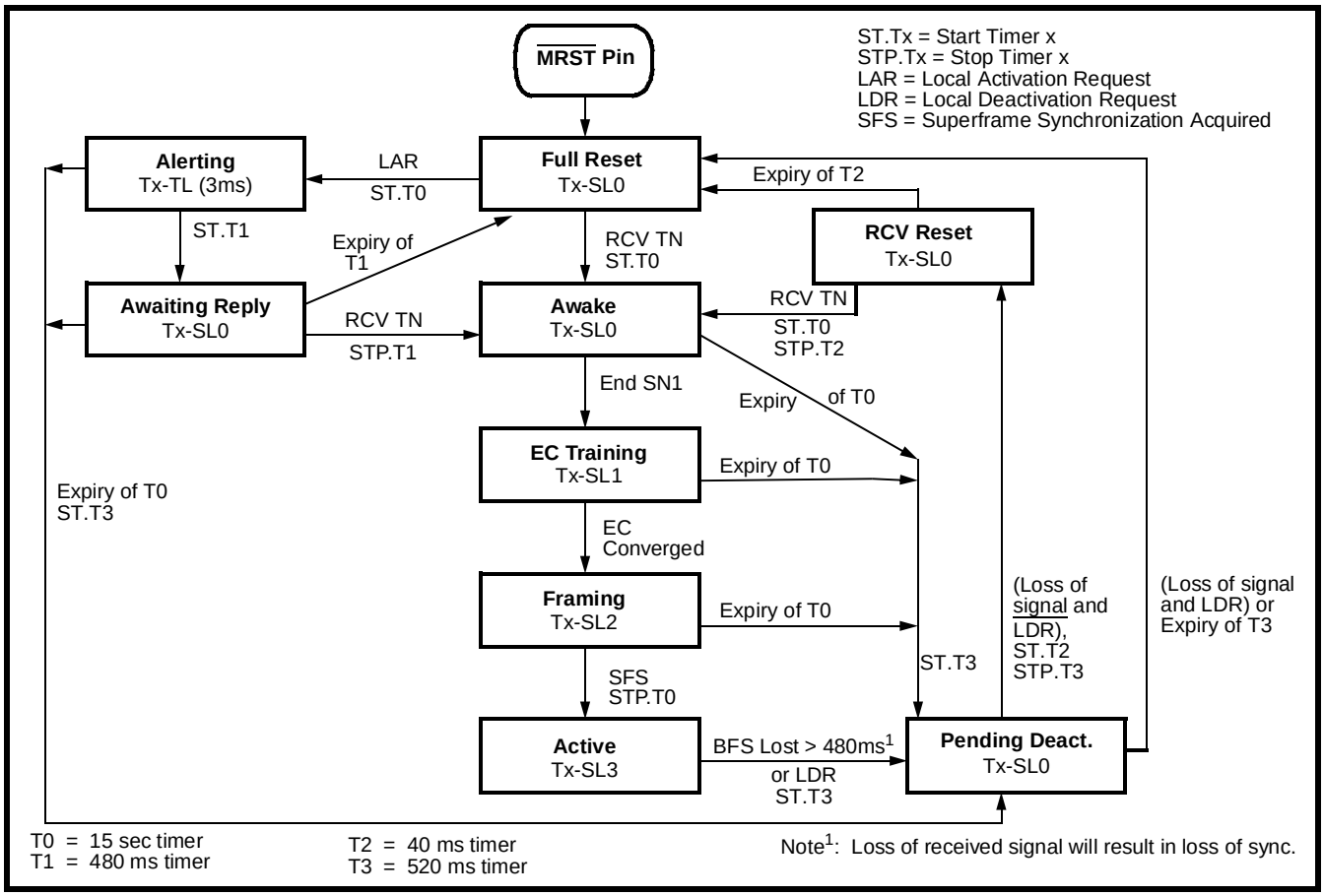


Figure 6a - Activation/Deactivation State Diagram - LT Mode

- TL: A 10 kHz activation tone sourced by the LT which is generated by sending a continuous pattern of four +3 symbols followed by four -3 symbols.
- SL0: SL0 is a no signal condition generated from the LT.
- SL1: An LT generated signal consisting of a framed (but not superframed), scrambled 2B1Q signal which carries all 1s in the B-, D- and M-channels. This signal is used to train the LT's echo canceller.
- SL2: An LT generated signal consisting of a fully framed and superframed scrambled 2B1Q signal which carries all 0s in the B- and D-channels with information in the M-channel. This signal is used to train the NT's DFE.
- SL3: An LT generated signal consisting of a fully framed and superframed scrambled 2B1Q signal which carries information in all the B-, D- and M-channels.

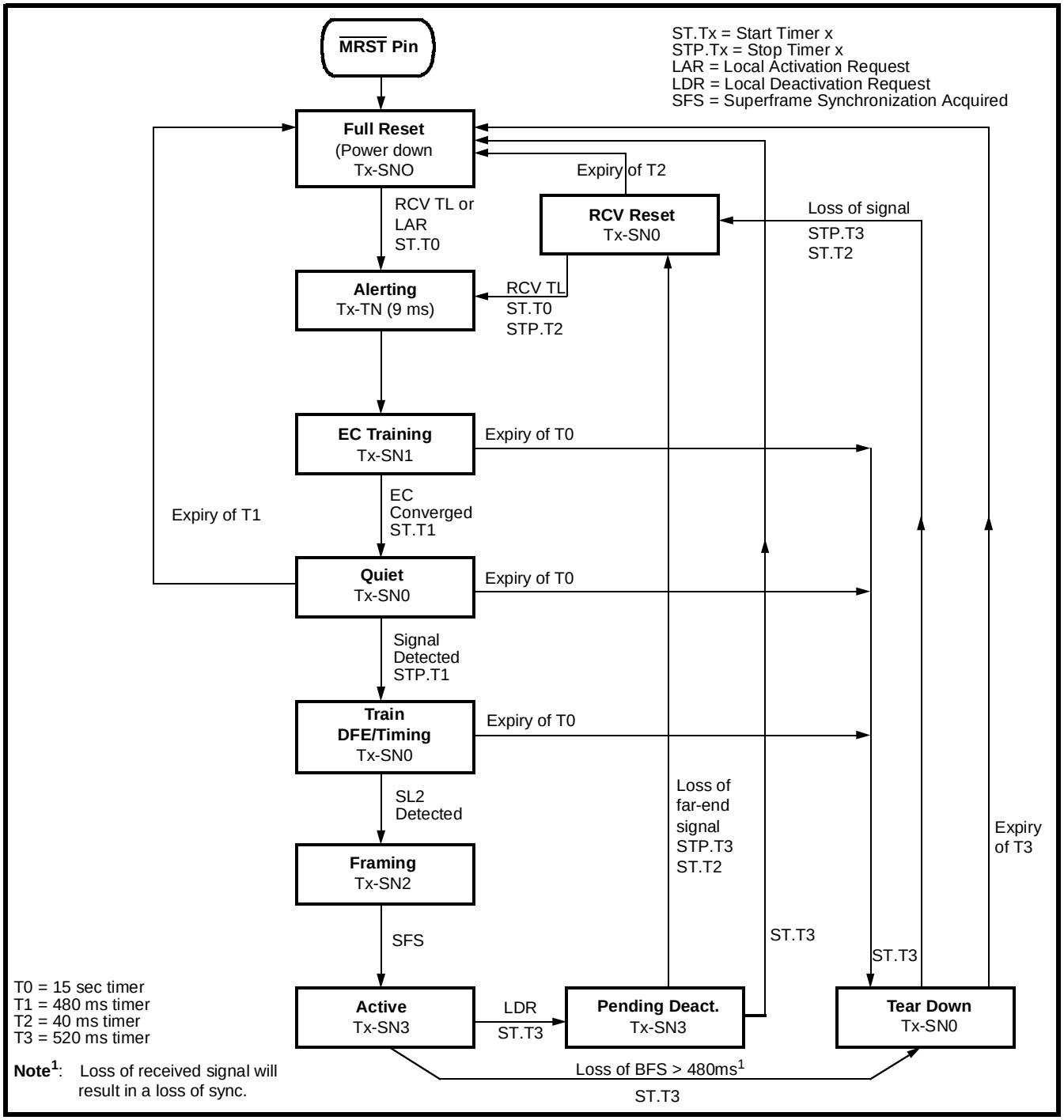


Figure 6b - Activation/Deactivation State Diagram - NT Mode

The reset state consists of two substates, the receive reset state and full reset state. The full reset state is entered following a power-up or after the expiry of the receive reset timer (40 ms). The receive reset state is a transient state which is entered once the DSLIC has detected a loss of received signal while the transceiver is not transmitting. In this state, the transceiver will not initiate the start-up sequence but is capable of responding to the appropriate activation tone. When the timer in the receive reset state has timed out (40 ms), the transceiver enters the full reset state.

All timers surrounding the reset states are included in the DSLIC and have been set as per the ANSI-T1.601-1988:

- Failure to complete a start-up sequence timer is set at 15 seconds.
- Loss of received signal timer is set at 480 ms as is the loss of synchronization.
- The receive reset state timer is set to 40 ms.
- A fourth timer (not specified in ANSI T1.601-1988) has been included which will restrict the time to 520 ms for a deactivation sequence.

The DSLIC will enter a deactivated state on the assertion of a deactivation request (setting the Start/ Stop bit to 0 in Control Register 1, and the subsequent loss of the received signal). Once the deactivation process has been completed, the request for activation can follow a warm start process as defined in ANSI T1.601-1988.

Loop Performance

The MT8910-1 operates on a digital subscriber line (DSL) which is a two wire twisted pair metallic medium typically used for transmission between the central office (LT) and the customer premise equipment (more commonly referred to as "Basic Access Interface on the Network side of the NT").

The MT8910-1 is production tested for error free performance for 2.5 sec (20,000 ST-BUS) frames over a 4.6km (15 kft) 26 AWG simulated loop (equivalent to 40dB attenuation @ 40 kHz).

ST-BUS Interface

The ST-BUS is a synchronous time division multiplexed serial bussing scheme with data streams operating at 2048 kbit/s configured as 32, 64 kbit/s channels (refer to Figure 7). Synchronization of the data transfer is provided from a frame pulse which identifies the frame boundaries and repeats at an 8 KHz rate. Figure 7 shows how the frame pulse ($\overline{F0b}$) defines the ST-BUS frame boundaries. All data is clocked into the device on the rising edge of the 4096 kHz clock ($\overline{C4b}$) three quarters of the way into the bit cell, while data is clocked out on the falling edge of the 4096 kHz clock at the start of the bit cell.

The bits on the ST-BUS are numbered bit 7 to bit 0 as outlined in Figure 7. Information transferred from the system port to the line port, will maintain the integrity of the bit order.

All timing signals, i.e., $\overline{F0b}$, $\overline{C4b}$ and $\overline{SFb}$, are bidirectional. The I/O configuration of these pins is controlled by the mode of operation (LT or NT). In the LT mode, these timing signals must be supplied from an external source and the MT8910-1 will in turn uses these timing signals to transfer information to and from the line port or the ST-BUS port. In the NT mode, timing is generated from an on board digital phase locked loop which extracts timing from the received data on the DSL and generates the system frame pulse ($\overline{F0b}$), the system 4096 kHz clock ($\overline{C4b}$) and the system superframe pulse ($\overline{SFb}$).

The superframe timing signal ($\overline{SFb}$) is an active low signal with a period of 12ms which is required to provide a reference for structuring the maintenance channel (M channel). In the LT mode, the $\overline{SFb}$ is an input which, when set low during the system frame pulse ($\overline{F0b}$), will set the phase of the transmit superframe. As an alternative, the $\overline{SFb}$ pin can be tied high and the device will automatically establish

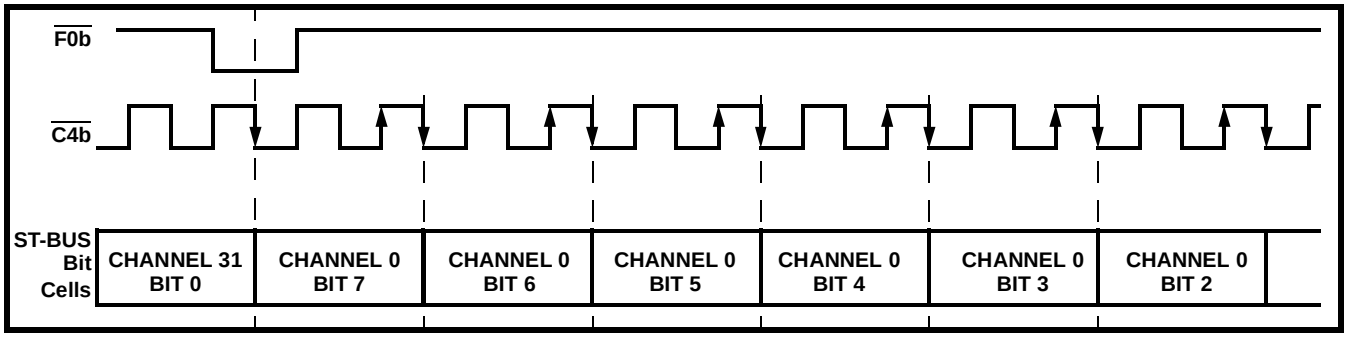


Figure 7 - ST-BUS Functional Timing

the superframe position. This function can also be activated in software (LT mode only) through a bit in Control Register 1 (TxSFB). The transition of this bit from a 1 to a 0 will reset the superframe counter, and the beginning of the transmitted superframe will be referenced to the ST-BUS frame after the frame in which the transition in the TxSFB bit occurred.

In the NT mode, the $\overline{SFb}$ pin is an output which generates an active low signal at the boundary of the transmit superframe. Since the $\overline{SFb}$ is referenced to the receive time base, $\overline{SFb}$ is only valid after superframe synchronization has been achieved. In the NT mode, the TxSFB bit is ignored since the transmit superframe has a fixed phase relationship with respect to the received superframe.

The MT8910-1 has two possible system port configurations; single port mode or dual port mode. In the single port mode, the MT8910-1 uses the first four timeslots of the DSTi and DSTo data streams (as shown in Figure 8). ST-BUS Channel 0 is allocated to the D-channel, ST-BUS Channel 1 to the C-channel, while ST-BUS Channel 2 and 3 are

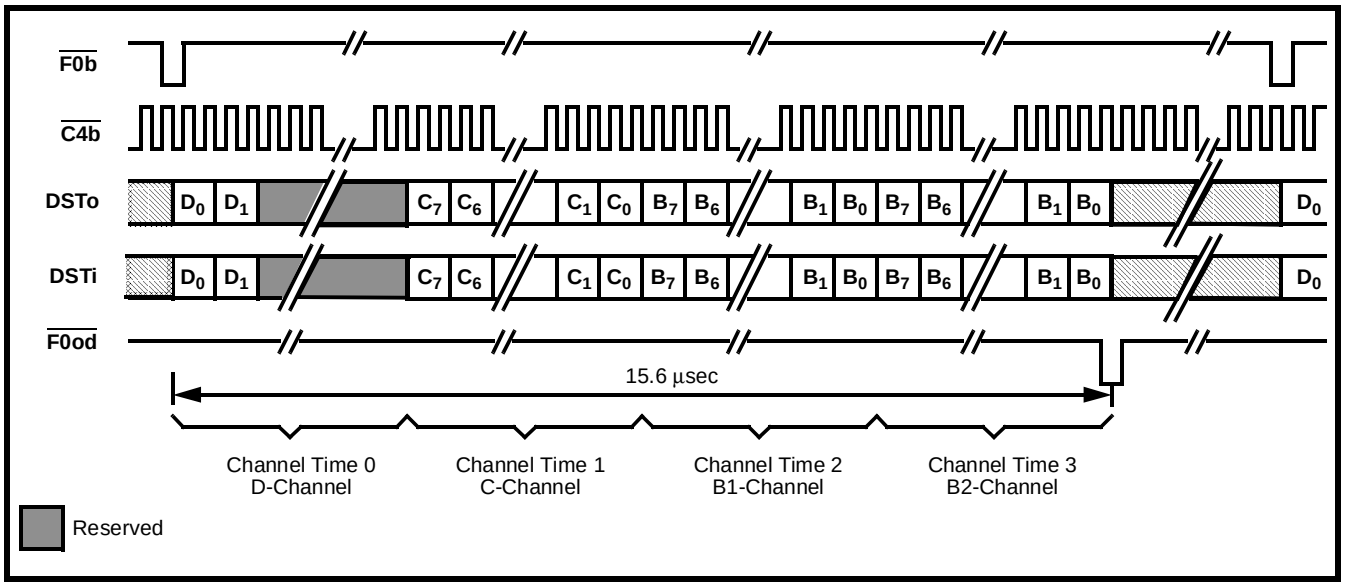


Figure 8 - ST-BUS Channel Assignments in Single Port Mode

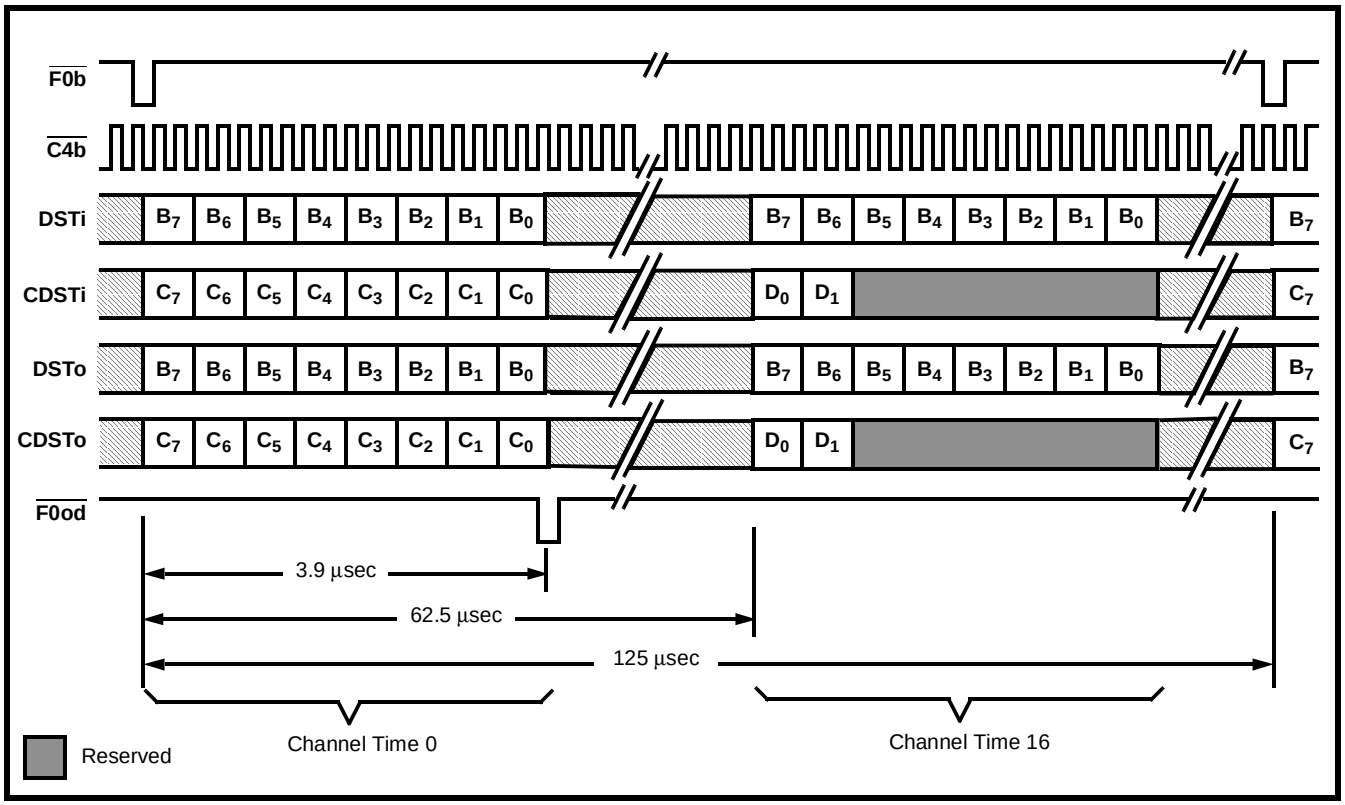


Figure 9 - ST-BUS Channel Assignment in Dual Port Mode

allocated to the B1 and B2 channels, respectively. In this mode, the CDSTi and CDSTo streams are not used. In the dual port mode, the MT8910-1 uses both the DSTi/DSTo streams as well as the CDSTi/CDSTo streams to allow the separation of the data and control. The two B-channels are routed through the DSTi/DSTo streams and the C- and D-channels are routed through the CDSTi/CDSTo streams. In each case, timeslot 0 and 16 will carry the respective channels (refer to Figure 9). To simplify line card designs, the MT8910-1 provides a delayed frame pulse (F0od) to eliminate the need for a channel assignment circuit. This signal is used to drive subsequent devices in the daisy chain configuration. In this type of arrangement, only the first MT8910-1 in the chain will receive the system frame pulse (F0b) with the following devices receiving its predecessor's delayed frame pulse. In conjunction with the delayed frame pulse, the unused timeslots on the ST-BUS will be placed into a high impedance state to avoid having contention on the system bus.

Selecting the single port or the dual port mode is performed using Mode Select 1 (MS1). With MS1=0, the DSLIC is in the single port mode while MS1=1 places the DSLIC in the dual port mode. Mode Select 0 (MS0) determines the order of the D- and C-channels while the DSLIC is operating in the dual port mode. With MS0 = 0, the C-channel is found in timeslot 0 and the D-channel is found in timeslot 16. With MS0=1, the D-channel is found in timeslot 0 and the C-channel is found in timeslot 16 (refer to Table 1).

MS1	MS0	Operating Mode	
		Dual/Single	DC/CD
0	0	Single	DC
0	1	Single	DC
1	0	Dual	CD
1	1	Dual	DC

Table 1. Truth Table for Mode Select Pins

Control/Status Channels

The Control and Status information between the DSLIC transceiver and the controlling entity is carried by the C-channel. The DSLIC has three input registers; Control Register 1, 2 and 3 (selected through the CRS0 and CRS1 bits) and four output registers; Status Register 1 through Status Register 4 (selected through the SRS0 and SRS1 bits in Control Register 1).

The input C-channel is used to access Control Registers 1, 2 and 3. Bit 0 and 1 of the C-channel (CRS0 and CRS1) allows the selection of the desired Control Register as described following.

CRS1	CRS0	Definition
0	0	Control Register 1
0	1	Control Register 2
0	0	Control Register 3
1	1	Reserved

The C-channel on the ST-BUS must be continuously written to every frame. If the user accesses a Control Register, the information in the other Control Registers is latched. Any input requested through the Control Registers will be activated on the next frame boundary.

Control Register 1

Setting CRS0 and CRS1=0 routes the C-channel to Control Register 1 allowing access to the functions described in Table 2. These bits are further described below.

Bits 7 and 6 of Control Register 1, SRS1 & SRS0, select which status register will be output in the next ST-BUS frame. The selection of the Status Register is as follows:

SRS1	SRS0	Definition
0	0	Status Register 1
0	1	Status Register 2
1	0	Status Register 3
1	1	Status Register 4

Bit 5 of Control Register 1, TxSFB, is used to establish the position of the transmit superframe (LT mode only). Setting this bit from a logic one to a logic zero will reset the frame counters on the next occurrence of the frame pulse establishing the superframe position. Once the boundaries to the superframe have been established, the device will sustain the position of the superframe by allowing the counters to wrap around. The user can also elect to set this bit to a logic zero with a periodicity of 12 ms.

Bit 4 of Control Register 1, BSWAP, allows the multiplexing of the two B-channels transferred over the digital subscriber line with the B-channels presented at the system interface. A logic high on the bit will result in the B1-channel on the system interface to be transmitted in the B2-channel on the line port and vice versa. The same principle applies to the B2-channel at the system interface.

Bit 3 of Control Register 1, CCRC, allows the user to introduce errors in the CRC bits calculated by the DSLIC. This allows the user to verify the error detection protocol used over the M-channel.

Bit 2 of Control Register 1, START/$\overline{\text{STOP}}$, provides a mechanism to allow the user to initiate a line activation or deactivation. This bit is edge sensitive with a low to high transition requesting an activation, and a high to low transition requesting a deactivation. The activation and deactivation procedure will follow the protocol defined in the ANSI T1.601-1988. The activation request will only be recognized if the transceiver is in a full reset state. Any activation attempt while the transceiver is in any other state will be ignored. Similarly, any deactivation request generated while the transceiver is not in the active state will be ignored.

Control Register 2

Setting CRS0=1 and CRS1=0 routes the C-channel to Control Register 2 allowing access to the functions described in Table 3. These bits are further described below.

Bits 7 to 4 of Control Register 2 (DS4 to DS1) provide access to the multiple diagnostic features supported on the DSLIC as outlined in Table 3. These include the per-channel loopbacks at the system interface as well as a loopback at the line interface. Along with the extensive loopback capabilities, the DSLIC also allows the generation of multiple signals which can be used during qualification and servicing of a DSL. The isolated pulse test diagnostics signal causes the transmission of a +3 or +1 symbol once every 1.5 ms. This will generate pulses that can be used for template measurements. The Insertion Loss Measurement (ILM) test signal is a scrambled all 1s 2B1Q coded signal which contain both the SW and ISW. This test signal can be used to make insertion loss measurements over the DSL loop. Lastly, the DSLIC can be placed into a quiet mode to allow a Remote Test Unit (RTU) to perform impulse noise, crosstalk and other transient impairment measurements as described in the ANSI "ISDN Management - Basic Rate Physical Layer".

Bit 3 of Control Register 2 (ADCGAIN) controls the gain value of the A/D converter. This function can be used to introduce more gain in the receive path when the transceiver is being used over long loops.

Bit 2 of Control Register 2 (MSWAP) may be used when the DSLIC is operating as an LT within a line card application. The mode swap feature has the effect of changing the scrambling polynomial and activation state machine such that it can simulate the operation of an NT transceiver. This allows a transmission test between two devices on the same line card. (For this function to work properly, the input clocks to the two devices must be frequency locked.)

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRS1	SRS0	TxSFB	BSWAP	CCRC	START/$\overline{\text{STOP}}$	CRS1	CRS0

Bit	Name	Description
7,6	SRS1, SRS0	Status Register Select. Selects which of the four status registers will be output in the next ST-BUS frame.
5	TxSFB	Transmit Superframe Reset. In LT mode, transition from a 1 to a 0 on this bit resets the superframe counters in the next ST-BUS frame in order to establish the transmit superframe boundary. If the external pin is being used to set the superframe boundary this bit can be held high or low. Not used in NT mode.
4	BSWAP	When this bit is set to 1, the location of the B1 channel on the ST-BUS is swapped with the location of the B2 channel. This affects both directions of the ST-BUS.
3	CCRC	Corrupt CRC. When set to 1, the 12 bit CRC transmitted on the line is corrupted.
2	START/$\overline{\text{STOP}}$	A low to high transition while the transceiver is in the full reset state will initiate one activation attempt. A high to low transition of this bit while the transceiver is in the active state will initiate a deactivation procedure. During start-up, 2B+D channels should remain set to 0 or 1 until transparency of network is achieved (indicated by act=1).
1, 0	CRS1, CRS0	Control Register Select 1 and 0. Must be set to 0, 0 to address Control Register 1.

Table 2. Control Register 1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
DS4	DS3	DS2	DS1	ADCGAIN	MSWAP	CRS1	CRS0

Bit	Name	Description
7,6, 5,4	DS4 - DS1	Diagnostic Select Bits.

DS4	DS3	DS2	DS1	Channels	Function
0	0	0	0	-	Normal Operation
0	0	0	1	B1	STi to STo Loopback [1]
0	0	1	0	B2	STi to STo Loopback [1]
0	0	1	1	B1 + B2	STi to STo Loopback [1]
0	1	0	0	2B + D	STi to STo Loopback [1]
0	1	0	1	B1	STo to STi Loopback [2]
0	1	1	0	B2	STo to STi Loopback [2]
0	1	1	1	B1 + B2	STo to STi Loopback [2]
1	0	0	0	2B + D	STo to STi Loopback [2]
1	0	0	1	ALL	L_{out} to L_{in} Loopback [1 3]
1	0	1	0	-	Isolated +3 pulse [4]
1	0	1	1	-	Isolated +1 pulse [4]
1	1	0	0	-	Transmit 10 kHz Tone
1	1	0	1	-	ILM Test Signal [5]
1	1	1	0	-	Quiet Mode
1	1	1	1	-	Reserved

3	ADCGAIN	Selects between two gain values in the delta-sigma A/D converter. When high, selects a 3 dB higher gain.
2	MSWAP	Mode Swap. In the LT mode, MSWAP=1 will result in the DSLIC using the NT's scrambling/ descrambling polynomials and activation sequence. This allows two DSLICs on the same LT line card to exchange static data in the B- and D- channels. MSWAP can also be used in the NT mode.
1, 0	CRS1, CRS0	Control Register Select 1 and 0. Must be set to 0, 1 respectively to address Control Register 2.

Table 3. Control Register 2

[1] The ST-BUS incoming data is still output on the line if the MT8910-1 is activated. Supported in both SINGLE and DUAL port modes.
[2] The incoming data from the line is still output on to the ST-BUS. The other incoming channels on the ST-BUS are still output on to the line if the device is activated. Supported in both SINGLE and DUAL port modes.
[3] Signal is internally looped back and is still output to the line and overrides the internal activation state machine.
[4] One pulse is transmitted every 1.5 ms.
[5] The Insertion Loss Measurement Test Signal is a scrambled (all one's data), framed 2B1Q signal.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
M1	M2	M3	M4	M5	M6	CRS1	CRS0

Bit	Name	Description
7 - 2	M1 - M6	Tx Maintenance Channel Bits 1 to 6. M-bits which will be transmitted at the end of the next DSL Basic Frame. Refer to "Maintenance Channel" section in the functional description
1, 0	CRS1, CRS0	Control Register Select 1 and 0. Must be set to 1, 0 respectively to address Control Register 3.

Table 4. Control Register 3

Control Register 3

Setting CRS1 and CRS0 to 1, 0, respectively, routes the input C-channel to Control Register 3, allowing access to the transmit M-bits as shown in Table 4. The transmit M-channel is a 4 kbit/s maintenance channel which may carry the EOC messages (with overhead) as specified in T1.601-1988. Except for the CRC bits, the M-bits are treated as a transparent data channel through the DSLIC. CRC bits will be generated by the transceiver and will be inserted into the M-channel during their respective M-bit time slots. (This implies that all input M-bits which are defined as CRC bits will be overwritten by the transceiver.) Structuring of the M-bits is described in the “Maintenance Channel" section of the functional description.

Control Words After Reset

Applying a logic low to the $\overline{\text{MRST}}$ pin will result in the three control registers assuming a reset state. Following a master reset, the three Control Registers will take the following states:

Control Register 1:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	1	0	0	0	0	0

Control Register 2:

C7	C6	C5	C4	C3	C2	C1	C0
0	0	0	0	0	0	0	1

Control Register 3:

C7	C6	C5	C4	C3	C2	C1	C0
1	1	1	1	1	1	1	0

Status Register 1

When SRID1=0 and SRID0=0, the contents of Status Register 1 are being output in the C-channel allowing the system to monitor the functions described below. (Refer to Table 5.)

Bits 7 and 6 of Status Register 1, SRID1 and SRID0, are used to identify which status register is being carried in the output C-channel. These bits are encoded as follows:

SRID1	SRID0	Definition
0	0	Status Register 1
0	1	Status Register 2
1	0	Status Register 3
1	1	Status Register 4

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRID1	SRID0	IS2	IS1	IS0	RxSFIB	RSV	CRCERR

Bit	Name	Description
7,6	SRID1, SRID0	Status Register ID. Always reads 0,0 when Status Register 1 is output.
5,4,3	IS2, IS1, IS0	Internal State Indication. **IS2 IS1 IS0 Definition** 0 0 0 Full Reset State 0 0 1 Training with no Basic Frame Sync 0 1 0 Training with Basic Frame Sync but no Superframe Sync 0 1 1 Training with Basic Frame Sync and Superframe Sync 1 0 0 Loss of synchronization after E.C. has converged 1 0 1 NA 1 1 0 Loss of superframe sync after E.C. has converged 1 1 1 Active State
2	RxSFIB	Received superframe Indication. When low, indicates the beginning of the received superframe. This bit is low for one ST-BUS frame, then high for 95 ST-BUS frames.
1	RSV	Reserved. Always read a 0.
0	CRCERR	When “1”, the received CRC code did not match with a locally generated CRC code, indicating that the received data included an error. When “0”, the received CRC code matched with the internally generated CRC.

Table 5. Status Register 1

Bits 5, 4 and 3 of Status Register 1, IS2, IS1 and IS0, provide an indication of the internal state of the device. The decoded states are as follows:

IS2	IS1	IS0	Definition
0	0	0	Full Reset
0	0	1	Training with no sync
0	1	0	Training with sync but no superframe sync
0	1	1	Training with sync and superframe sync
1	0	0	Loss of sync
1	0	1	NA
1	1	0	Loss of superframe sync
1	1	1	Active

Bit 2 of Status Register 1, RxSFIB, is used to indicate the reception of the receive superframe boundary in both the LT and NT modes.

Bit 0 of Status Register 1, CRCERR, indicates the state of the CRC check. A logic high on this bit states that the CRC check calculated by the MT8910-1 did not correspond to the CRC bits received in the M-channel. This bit will only be updated once every superframe.

Status Register 2

When SRID1=0 and SRID0=1, the contents of Status Register 2 are being output in the C-channel allowing the system to monitor the status of the quantizer signal to noise ratio bits (refer to Table 6). The QSNR bits reflect the eye closure of the received signal and represent the signal (+1 symbol) to noise ratio at the input of the quantizer. This information can be used to indicate the error performance of the transceiver. For a more accurate indication of QSNR, these bits should be averaged over a period of 64 ST-BUS frames (640 baud). The conversion of the five bit output to QSNR is shown in Table 6. For a bit error rate of greater than 10^{-7}, the theoretical QSNR should be greater than 15.7dB.

Status Register 3

When SRID1=1 and SRID0=0, the contents of Status Register 3 are being output in the C-channel allowing the system to monitor the mean level of the received symbols (refer to Table 7). The Received Pulse Amplitude bits (RPA4 to RPA0) provide an estimate of the attenuation of the loop. The representation of the RPA bits is shown in Table 7.

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRID1	SRID0	QSNR4	QSNR3	QSNR2	QSNR1	QSNR0	NA

Bit	Name	Description
7,6	SRID1, SRID0	Status Register ID. Always reads 0, 1, respectively, when Status Register 2 is output.
5,4,3, 2,1	QSNR4, QSNR3, QSNR2, QSNR1, QSNR0	Quantizer Signal to Noise Ratio Bits. (see Note 1)
0	NA	Reserved. Always reads 0.

QSNR4 (MSB) - QSNR0 (LSB)	MEAN QSNR (dB)	QSNR4 (MSB) - QSNR0 (LSB)	MEAN QSNR(dB)
00000	>36.1	10000	12.1
00001	36.1	10001	11.5
00010	30.1	10010	11.0
00011	26.6	10011	10.6
00100	24.1	10100	10.1
00101	22.2	10101	9.7
00110	20.6	10110	9.3
00111	19.2	10111	8.9
01000	18.1	11000	8.5
01001	17.1	11001	8.2
01010	16.1	11010	7.9
01011	15.3	11011	7.5
01100	14.6	11100	7.2
01101	13.9	11101	6.9
01110	13.2	11110	6.6
01111	12.6	11111	6.3

Table 6. Status Register 2

Note 1) Not Production Tested

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRID1	SRID0	RPA4	RPA3	RPA2	RPA1	RPA0	RSV

Bit	Name	Description
7,6	SRID1, SRID0	Status Register ID. Always reads 1, 0, respectively, when Status Register 3 is output.
5,4,3, 2,1	RPA4-RPA0	Receive Pulse Amplitude bits (see Note 1).

RPA4 - RPA0	Relative Amplitude (dB)	RPA4 - RPA0	Relative Amplitude (dB)
0 0 0 0 0	-31.85	1 0 0 0 0	-7.76
0 0 0 0 1	-30.10	1 0 0 0 1	-6.02
0 0 0 1 0	-28.65	1 0 0 1 0	-4.57
0 0 0 1 1	-27.41	1 0 0 1 1	-3.33
0 0 1 0 0	-25.83	1 0 1 0 0	-1.74
0 0 1 0 1	-24.08	1 0 1 0 1	0
0 0 1 1 0	-22.63	1 0 1 1 0	1.45
0 0 1 1 1	-21.39	1 0 1 1 1	2.69
0 1 0 0 0	-19.80	1 1 0 0 0	4.28
0 1 0 0 1	-18.06	1 1 0 0 1	6.02
0 1 0 1 0	-16.61	1 1 0 1 0	NA
0 1 0 1 1	-15.37	1 1 0 1 1	NA
0 1 1 0 0	-13.78	1 1 1 0 0	NA
0 1 1 0 1	-12.04	1 1 1 0 1	NA
0 1 1 1 0	-10.59	1 1 1 1 0	NA
0 1 1 1 1	-9.35	1 1 1 1 1	NA

Notes: Loop length can be calculated by dividing Receive Pulse Amplitude (RPA) by the typical cable attenuation for a 2B1Q pulse.
Relative amplitude is based on RPA reading of zero line length with recommended termination and transformer (ADC Gain = 0).

0	RSV	Reserved. Always reads 0.

Table 7. Status Register 3

Note 1) Not Production Tested

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
SRID1	SRID0	M1	M2	M3	M4	M5	M6

Bit	Name	Description
7,6	SRID1, SRID0	Status Register ID. Always reads 1, 1, respectively, when Status Register 4 is output.
5,4,3, 2,1,0	M1 - M6	Rx Maintenance Channel Bits 1 to 6. M-bits which were received at the end of the last DSL Basic Frame. Refer to the "Maintenance Channel" section in the functional description for the structuring of the received M-bits.

Table 8. Status Register 4

ST-BUS Frame Access	M1	M2	M3	M4	M5	M6
0 - 9	M11	M21	M31	M41	M51	M61
12 -21	M12	M22	M32	M42	M52	M62
24 - 33	M13	M23	M33	M43	CRC1	CRC2
36 - 45	M14	M24	M34	M44	CRC3	CRC4
48 - 57	M15	M25	M35	M45	CRC5	CRC6
60 - 69	M16	M26	M36	M46	CRC7	CRC8
72 - 81	M17	M27	M37	M47	CRC9	CRC10
84 - 93	M18	M28	M38	M48	CRC11	CRC12

Table 9. Maintenance Channel Bit Assignment on ST-BUS Port

Status Register 4

When SRID1=1 and SRID0=1, the contents of the Status Register 4 are being output in the C-channel allowing the system to monitor the received maintenance channel bits M1 to M6 as specified in Table 8. The received M-bits may carry the EOC message (with overhead) as specified in T1.601-1988. Refer to the “Maintenance Channel“ section for further details.

Maintenance Channel

The MT8910-1 has provisions for transmitting and receiving a 4 kbit/s maintenance channel from the system port to the line port. The maintenance channel at the line port is structured into six columns of which M5 and M6 carry the results of a CRC calculation (refer to Table 9). All bits except these CRC bits are treated as a transparent channel to the MT8910-1. The 12 bit cyclical redundancy check is computed using the generator polynomial:

$$x^{12} \oplus x^{11} \oplus x^3 \oplus x^2 \oplus x \oplus 1$$

(where $\oplus$ is modulo two summation)

The CRC calculation covers all 2B + D-channels within a superframe as well as the M4 column within the maintenance channel.

Access to the maintenance channel is granted through Control Register 3 (Tx M-Channel) and Status Register 4 (Rx M-Channel) and is structured on the ST-BUS port as shown in Table 9. The Tx M-bits for all DSL basic frames are written to Control Register 3 once every 1.5ms within the ST-BUS frames indicated in Table 9. If the user fails to update the contents of Control Register 3 within the allocated window, the M-bits will be substituted by ones until the information in Control Register 3 is updated. On the receive path, the Rx M-bits from each DSL basic frame are available in Status Register 4 within the ST-BUS frames indicated in Table 9. The Rx M-bits will be updated every DSL basic frame (or 1.5 ms).

The M-bits are structured according to the transmit and receive superframe boundary signals output on the ST-BUS. The transmit superframe boundary is defined relative to the input or output $\overline{SFb}$ signal. (In LT mode, the transmit superframe boundary can also be defined in the frame following the TxSFB bit being set to zero.) The ST-BUS frame in which the $\overline{SFb}$ signal is active is defined as transmit frame 0. The superframe boundary in the receive path is defined relative to the RxSFIB bit found in Status Register 1. The ST-BUS frame with RxSFIB=0 is defined as the receive frame 0. The functional timing diagram for the phase of the $\overline{SFb}$ and RxSFIB signals for both the LT and NT modes is shown in Figure 10.

In applications which do not utilize the maintenance channel, 2B+D data at the NT and the LT should be all set to 0 or 1 until activation occurs at the LT. Since the NT trains up before the LT, the activation at the LT can be detected at the NT by the reception of random data. Only then the NT can transmit normal 2B+D data.

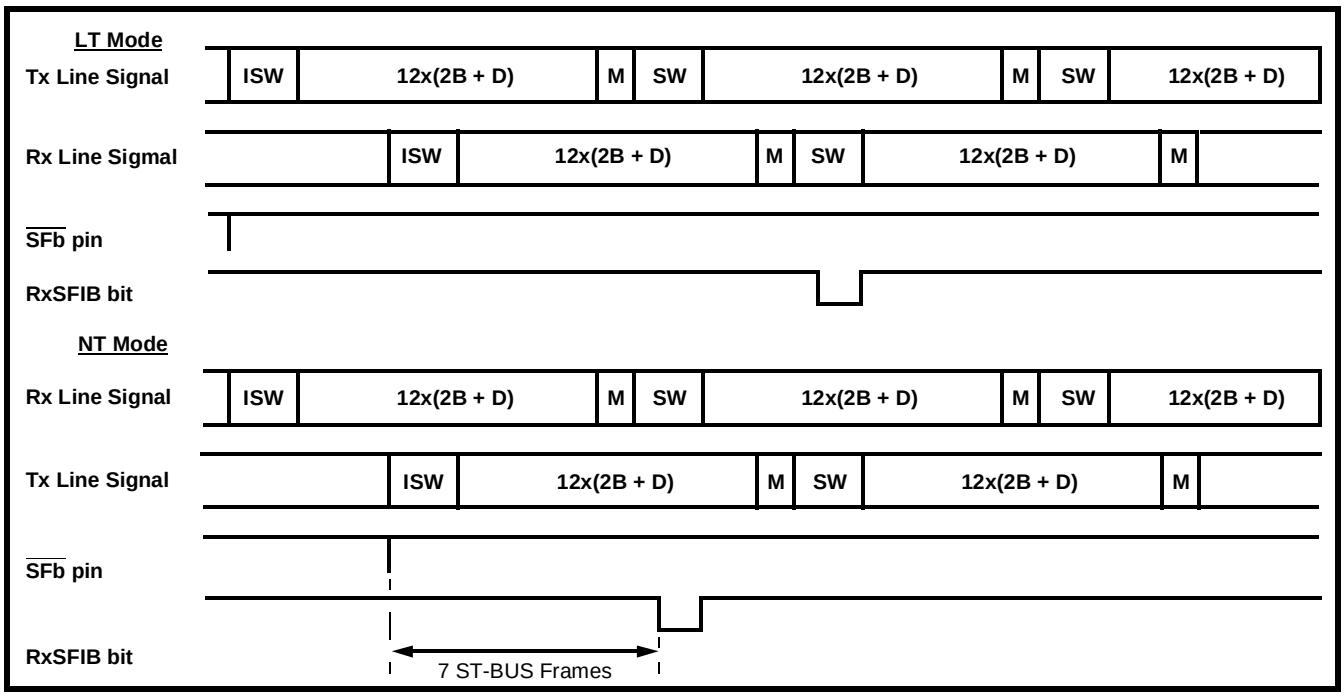


Figure 10 - Functional Timing for Superframe Signals

10.24 MHz Clock Interface

The MT8910-1 can operate either with an external clock or with a built-in oscillator clock using a 10.24 MHz parallel resonance crystal. While using the external clock, the timing relationship between $\overline{C4b}$ and the external clock should be as shown in Figure 15. This is typically used in LT mode. To meet the specified line performance, the tolerance of the external clock should be ±5ppm. In NT mode, the MT8910-1 can use the built-in crystal oscillator circuit for internal timing, and to meet the specified line performance, the tolerance of the crystal is specified to be ±50ppm.

The oscillator in the MT8910-1 uses the Pierce circuit configuration. In this type of oscillator, the necessary phase shift is obtained by the two components connected in series; one of them is the crystal itself, and the other is the RC combination of the output impedance of the inverter and the capacitor connected to its output and the ground. This requires the output impedance of the inverter to be high for minimizing the power consumption of the MT8910-1. When OSC1 is used as an input for an external clock (typically in LT mode), the high output impedance of the inverter coupled with any stray capacitance on the OSC2 pin can distort the waveform and change the duty cycle of the clock signal fed to the internal blocks of the MT8910-1. This may result in improper operation. Hence, it is recommended that an external inverter be connected in parallel strengthening the internal inverter as shown in Figure 11.

I/O Structure Test

The MT8910-1 has a built-in test structure that allows verification of all digital I/O structures. The "I/O Structure Test" is a static test designed to allow a parity check on all digital inputs, force all digital output drivers to any state as well as placing all digital outputs into a high impedance state. These three variables can be used to verify the integrity of the connections between the MT8910-1 and the printed circuit board.

The I/O structure test has three dedicated pins which are used to; enable the test structure (TSTen), provide an output (TSTout) of an XOR chain that is used to verify all digital input pins, as well as providing an input signal (TSTin) to all output drivers. Before enabling the test structure, the default I/O structure must be cleared to avoid interference with the test results. This can be accomplished by inserting the test vectors as defined in Table 10 below. Once the initialization procedure has been run, the respective testing mode can be enabled using the three mode select pins MS0, MS1 and NT/$\overline{LT}$.

The I/O structure test allows the verification of the connection between the printed circuit board and the digital input pins to the MT8910-1. After running the initialization sequence described above, the I/O input structure test can be enabled by setting TSTen to a logic high with the mode select pins MS0, MS1 and NT/$\overline{LT}$ set to 1, 0, 1 respectively. This forces all digital inputs to be linked into an XOR chain whose output drives the I/O structure test output (TSTout) pin[1]. The TSTout pin will carry the output of the XOR comparison from signals on pins, CDSTi, DSTi,

		Initialization							Input Tests							Output Tests				
Time Stamp (e.g.: 1 µs)		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Input Signals	**TSTen**	0	0	0	0	0	0	0	1	1	•	•	•	1	1	0	1	1	1	1
	MS0	0	0	0	0	0	0	0	1	1	•	•	•	1	1	0	1	1	1	1
	MS1	0	0	0	0	0	0	0	0	0	•	•	•	0	0	0	1	1	1	0
	NT/$\overline{LT}$	0	0	0	0	0	0	0	1	1	•	•	•	1	1	0	0	0	0	0
	TSTin	0	0	0	0	0	0	0	0	0	•	•	•	0	0	0	0	1	0	0
	CDSTi	0	0	0	0	0	0	0	0	1	•	•	•	0	0	0	0	0	0	0
	$\overline{DSTi}$	0	0	0	0	0	0	0	0	0	•	•	•	0	0	0	0	0	0	0
	$\overline{MRST}$	0	0	0	0	0	0	0	0	0	•	•	•	0	0	0	0	0	0	0
	OSC1	0	1	0	0	0	0	0	0	0	•	•	•	0	0	0	1	0	1	0
Output Signals	**DSTo**	X	X	X	X	X	X	X	X	X	•	•	•	X	X	X	0	1	0	Z
	CDSTo	X	X	X	X	X	X	X	X	X	•	•	•	X	X	X	0	1	0	Z
	$\overline{F0od}$	X	X	X	X	X	X	X	X	X	•	•	•	X	X	X	0	1	0	Z
	OSC2	X	X	X	X	X	X	X	X	X	•	•	•	X	X	X	0	1	0	1
	TSTout	X	X	X	X	X	X	X	L	H	•	•	•	L	H	X	0	1	0	Z
Bidirectional Signals	**$\overline{C4b}$**	0	1	0	0	1	0	1	0	0	•	•	•	0	0	X	0	1	0	Z
	$\overline{F0b}$	0	0	0	1	1	1	0	0	0	•	•	•	0	0	X	0	1	0	Z
	$\overline{SFb}$	0	0	0	0	0	0	0	0	0	•	•	•	0	1	X	0	1	0	Z

Table 10. I/O Structure Test Vectors

X=Don't Care Z=High Impedance State

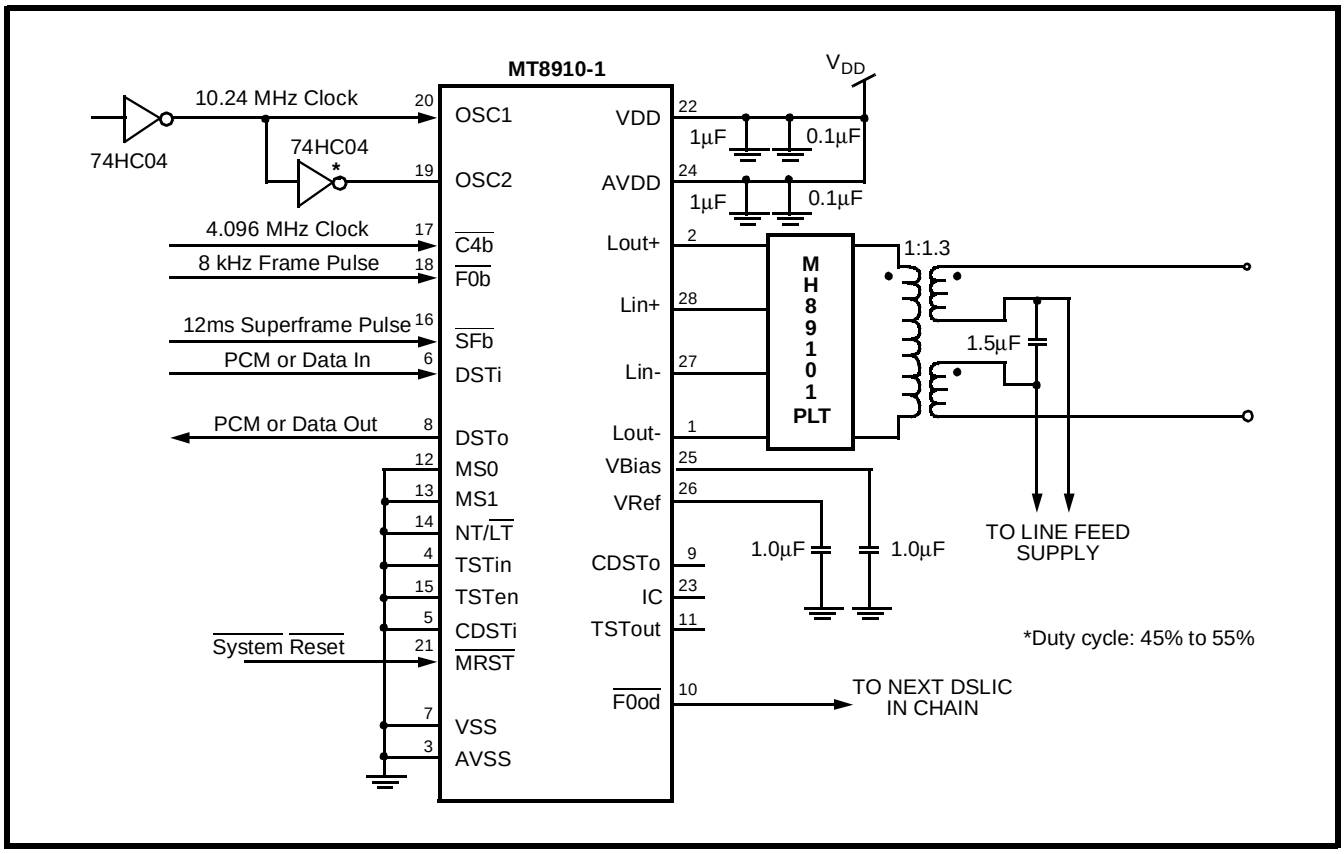


Figure 11 - Typical Connections for LT Mode (Single Port)

$\overline{\text{MRST}}$, OSC1, $\overline{\text{C4b}}$, $\overline{\text{F0b}}$ and $\overline{\text{SFb}}$. TSTout=0 if all input signals carry an even number of ones and TSTout=1 if all input signals carry an odd number of ones.

The I/O structure test also allows the verification of the connection between the digital output pins and the printed circuit board. After running the initialization sequence, the I/O structure output test can be enabled by setting the TSTen to a logic high with the mode select pins MS0, MS1 and NT/$\overline{\text{LT}}$ set to 1, 1, 0 respectively. This causes all digital outputs to be driven from the I/O structure test input (TSTin) pin1. The outputs affected include the DSTo, CDSTo, $\overline{\text{F0od}}$ and TSTout

These same outputs can also be placed into a high impedance state to allow the bed-of-nails tester or some other in-circuit tester to drive a known signal or pattern on any circuitry that may be connected to the output pins of the MT8910-1. The high impedance state is enabled by running the initialization pattern described above then setting TSTen to a logic one with the mode select pins MS0, MS1 and NT/$\overline{\text{LT}}$ set to 1, 0, 0 respectively.

Note [1]: Allow a propagation delay of approximately 800ns from digital input to XOR output or TSTin to any digital output.

Applications

The typical connection diagrams are shown in Figures 11 and 12. In Figure 11, the MT8910-1 receives all its timing from the system including the $\overline{\text{C4b}}$, $\overline{\text{F0b}}$ and a frequency-locked 10.24 MHz master clock. In Figure 12, the MT8910-1 is configured in the NT mode which implies that all timing signals including the $\overline{\text{F0b}}$, $\overline{\text{C4b}}$ and $\overline{\text{SFb}}$ are being sourced from the MT8910-1. These timing signal are generated from an internal DPLL which divides a 10.24 MHz reference frequency down to a baseband 160 kHz. A comparison is performed on the reference signal with the received line signal to determine if the timing signals on the MT8910-1 have to be corrected.

The MT8910-1 is interfaced to the transmission line through the Passive Line Termination network (PLT) and transformer. The PLT provides the two to four wire conversion and additional frequency compensation for the received signal. The whole circuit is DC isolated from the line by the low inductance transformer.

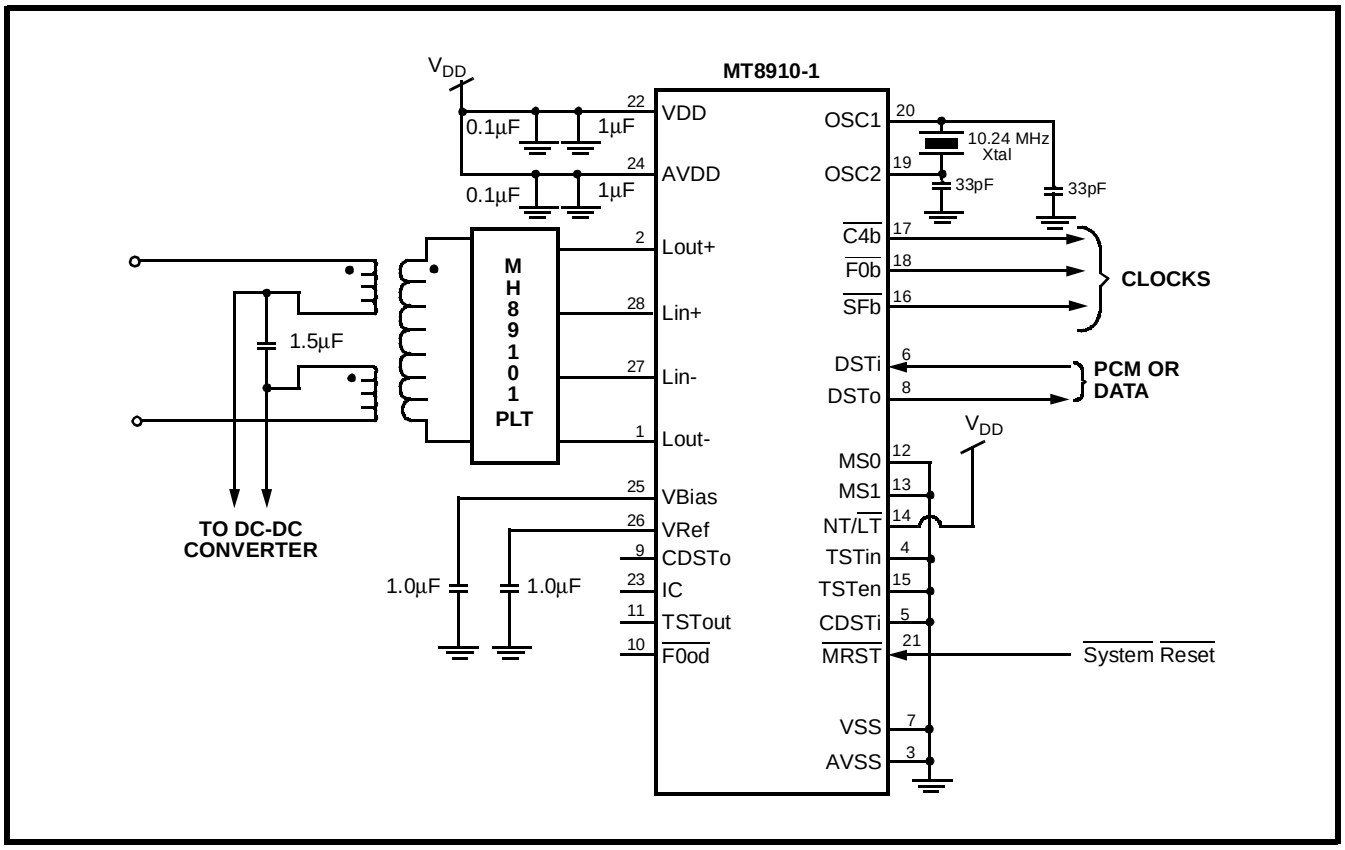


Figure 12 - Typical Connections for NT Mode (Single Port)

Passive Line Termination Network (PLT)

The termination network is an all passive circuit which allows the MT8910-1 to interface to the DSL line through a line pulse transformer. The passive line termination consists of three blocks which includes a hybrid network, a compensator circuit and a line pulse transformer (refer to Figures 13 and 14).

The hybrid network is a 2 to 4 wire converter which provides limited precancellation of near end echo. The hybrid specified in Figure 13 was optimized for the specified transformer and a 10 ohm series protection resistor (Rp).

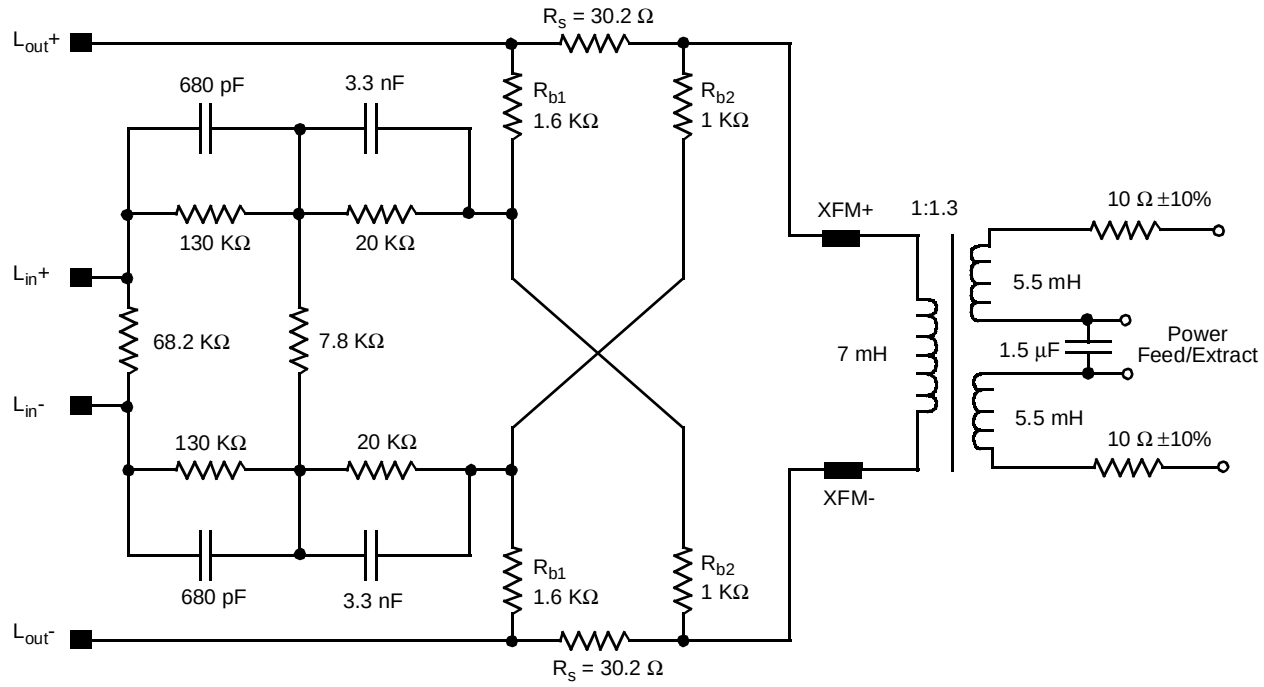
The compensator circuit, in conjunction with the transformer, acts as a high pass filter which is designed to increase the cut-off frequency in the receiver path. This has the effect of reducing the low frequency content in the received line signal which in turn reduces the effects of ISI and near end echo thereby improving transceiver performance.

The low inductance transformer allows for the possibility of passing a sealing current and/or phantom feed supply through the secondary winding without saturating the magnetic core. The transformer specified in Figure 14 has been designed to carry typically 50 mA of DC current.

Transformer Specification

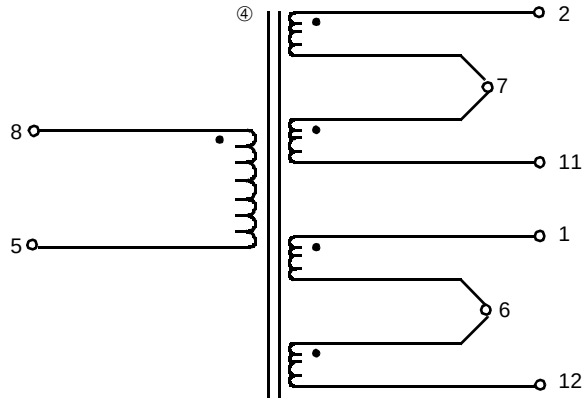
All subscriber equipment which is to be connected to a digital subscriber line, must deliver an output pulse which satisfies both the pulse template and the pulse PSD as specified earlier. The output drive characteristics of the MT8910-1 requires a transformer with a turns ratio of 1:1.3 having the electrical characteristics specified in Figure 14.

For supporting initial design activities, Mitel Semiconductor has made available the MB6024 Magnetic Kit which contains the transformer shown in Fig. 14.



Note 1: All resistors have a tolerance of ±1% unless indicated otherwise. All capacitors have a tolerance of ±10%.
Note 2: May be incorporated on to a ceramic substrate.

Figure 13 - Passive Line Termination (PLT)



TURNS RATIO	1:1.3	
RESISTANCE	R_1 = 5-8	3.7 Ω
	R_2 = 2-12	6.8 Ω ③
INDUCTANCE	L_P = 5-8	7 mH ①
	L_S = 2-12	11 mH ② ③
Leakage Inductance (Sec. Short Circuit) < 75µH @ 40 kHz.		
LONGT. BAL.	0 - 4 kHz	min 63 dB
	4-160 kHz	min 58 dB

NOTES:
① Open Circuit Secondary
② Open Circuit Primary
③ With pins 1 and 11 shorted together
④ Filtran Part Number TPW 4671

Figure 14 - Transformer Specification

Absolute Maximum Ratings*

	Parameters	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any I/O pin	$V_{I/O}$	-0.3	V_{DD} +0.3	V
3	Current on any I/O pin	$I_{I/O}$		20	mA
4	Storage Temperature	T_{ST}	-55	125	°C
5	Package Power Dissipation	P_D		1000	mW

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Note 1: Except for V_{DD}, AV_{DD}, V_{SS}, AV_{SS}, L_{out+} and L_{out-}.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.00	5.25	V	(see Note 1)
2	Analog Supply Voltage	AV_{DD}	4.75	5.00	5.25	V	Relative to AV_{SS} (Note 1)
3	Input Low Voltage (except OSC1, MRST, MS0, MS1, NT/LT	V_{IL}			0.4		for 400mV noise margin
4	Input High Voltage (except OSC1, MRST, MS0, MS1, NT/LT	V_{IH}	2.4			V	for 400mV noise margin
5	Input Low Voltage for OSC1/2, MRST, MS0, MS1, NT/LT	V_{IL}			1.0	V	
6	Input High Voltage for OSC1/2, MRST, MS0, MS1, NT/LT	V_{IH}	4.0			V	
7	Operating Temperature	T_A	0		70	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note 1: To obtain optimum line performance, noise level on supply must be less than 25 mVpp.

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	INPUTS	Input High Voltage (except OSC1, MRST, MS0, MS1, NT/LT	V_{IH}	2.0			V	
2		Input Low Voltage (except OSC1, MRST, MS0, MS1, NT/LT	V_{IL}			0.8	V	
3		Input High Voltage for OSC1/2, MRST, MS0, MS1, NT/LT	V_{IH}	3.0			V	
4		Input Low Voltage for OSC1/2, MRST, MS0, MS1, NT/LT	V_{IL}			2.0	V	
5		Input Leakage Current (except OSC1)	I_{IL}			10	µA	$V_{IN} = V_{SS}$ to V_{DD}
6		Input Current for OSC1	I_{IC}		50	100	µA	$V_{IN} = V_{SS}$ to V_{DD}
7		Input Impedance (L_{in-} to L_{in+})	Z_{in}		250		kΩ	@ DC

DC Electrical Characteristics (continued) - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
8		V_{Bias} Voltage	V_{Bias}		$0.5AV_{DD}$		V	Relative to AV_{SS} C_L=1 µF minimum to AV_{SS}
9		V_{Ref} Voltage	V_{Ref}		-1.9		V	Relative to V_{Bias} C_L= 1µF minimum to AV_{SS}
10		V_{Bias} and/or V_{Ref} load	V_{BL}	1			MΩ	(see Note 2)
11		Output High Voltage(1)	V_{OH}	2.4			V	I_{OH}=10mA
12		Output Low Voltage (1)	V_{OL}			0.4	V	I_{OL}= 5.0mA
13	OUTPUTS	OSC2 Output High Voltage	V_{OH}		3.5		V	I_{OH}=10µA
14		OSC2 Output Low Voltage	V_{OL}		1.5		V	I_{OL}=10µA
15		Differential Output Voltage (L_{out+} to L_{out-})	V_{out}		6.4		V_{pp}	R_L=40Ω
16		Output Impedance (L_{out+}, L_{out-})	Z_{out}		0.5		Ω	Measured by sourcing and sinking 10 mA. Line Driver active.
17		Output Capacitance (L_{out+}, L_{out-})	C_o			50	pF	(see Note 1)
18		High Impedance Leakage	I_{OZ}			10	µA	
19		Supply Current	I_{DD} I_{DD}		65 10		mA mA	Line Drivers active and unloaded. Low Power Mode

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
(1) except OSC2
Note 1) This is a specification on the maximum parallel capacitance to AC ground, connected directly to the pins. Higher capacitance is acceptable when placed in series with resistor networks such as the line termination impedance.
2) Not production tested.

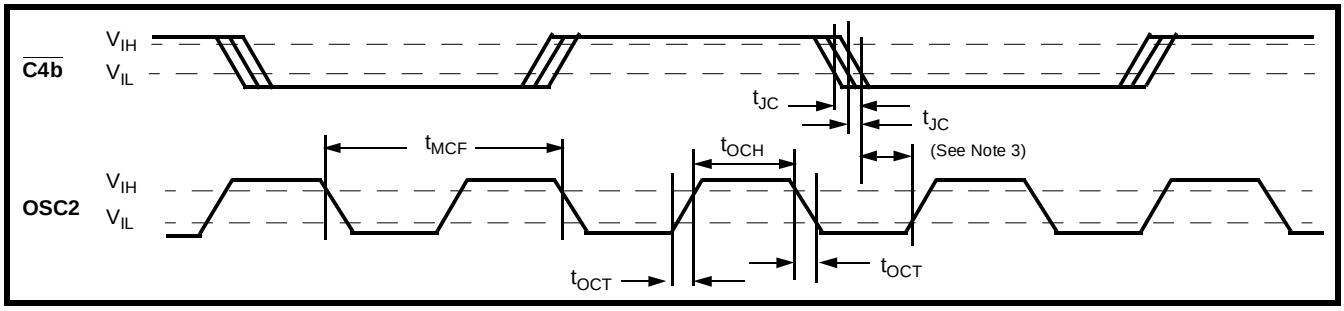


Figure 15 - External Clock Timing in LT Mode

AC Electrical Characteristics† - External Clock Timing (Ref. Figure 15)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	OSC2 Clock Frequency	$1/t_{MCF}$		10.24		MHz	(see Notes 1, 2 & 3)
2	OSC2 Clock Duty Cycle	t_{OCH}/t_{MCF}	45	50	55	%	
3	OSC2 Clock Transition Time	t_{OCT}			10	ns	
4	$\overline{C4b}$ Jitter (wrt OSC2)	t_{JC}	-15		+15	ns	(see Note 3)

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Notes: 1) External clock tolerance of ±5 ppm in LT mode or ±50 ppm in NT mode is required.
2) Absolute jitter on OSC2 must be less than 2.0ns RMS in order to maximize performance.
3) In LT mode the $\overline{C4b}$ and OSC2 clocks must be externally frequency locked (i.e., f_{OSC2} = 2.5 x f_{C4b}). The relative phase between the clocks is not critical.

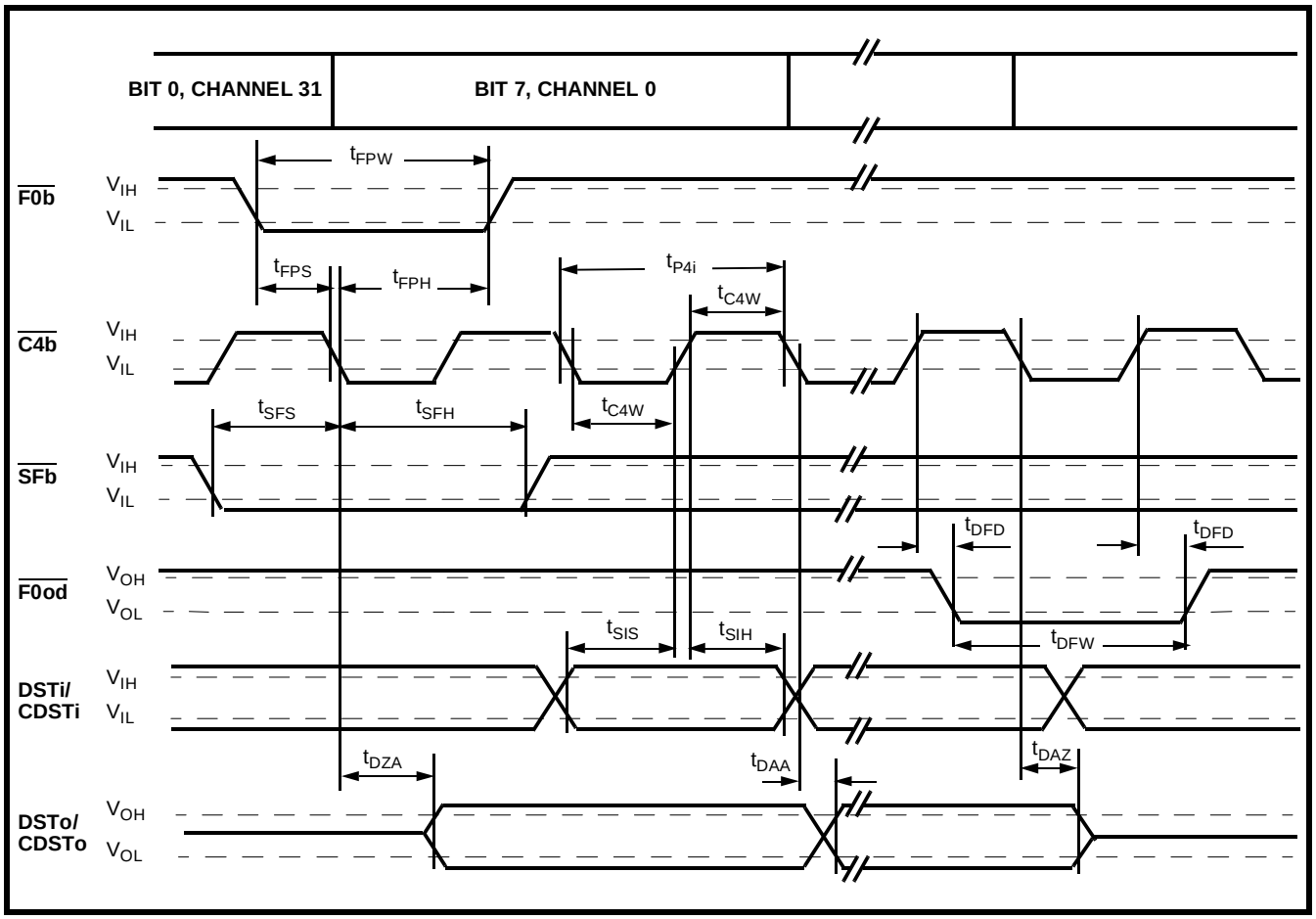


Figure 16 - ST-BUS Timing LT Mode

AC Electrical Characteristics† - ST-BUS Timing LT Mode (Ref. Figure 16)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{\text{F0b}}$ Input Pulse Width	t_{FPW}		244		ns	
2	Frame Pulse ($\overline{\text{F0b}}$) Setup Time	t_{FPS}	50			ns	(see Note 2)
3	Frame Pulse ($\overline{\text{F0b}}$) Hold Time	t_{FPH}	50			ns	(see Note 2)
4	$\overline{\text{C4b}}$ Input Clock Period	t_{P4i}		244		ns	
5	$\overline{\text{C4b}}$ Pulse Width High or Low	t_{C4W}		122		ns	
6	Superframe Setup Time	t_{SFS}	50			ns	(see Note 2)
7	Superframe Hold Time	t_{SFH}	50			ns	(see Note 2)
8	$\overline{\text{F0od}}$ Delay	t_{DFD}			60	ns	150 pF Load (see Notes 1 & 2)
9	$\overline{\text{F0od}}$ Pulse Width	t_{DFW}		244		ns	150 pF Load (see Note 1)
10	Serial Input Setup Time	t_{SIS}	30			ns	(see Notes 1 & 2)
11	Serial Input Hold Time	t_{SIH}	50			ns	(see Notes 1 & 2)
12	Serial Output Delay Act to Act High Z to Act Act to High Z	t_{DAA} t_{DZA} t_{DAZ}			120 120 120	ns	150 pF Load (see Notes 1 & 2) 150 pF Load (see Notes 1 & 2) 150 pF Load (see Notes 1 & 2)

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
Note 1) These timing parameters are mode independent (NT or LT).
2) Tested @ 5V, 25°C only.

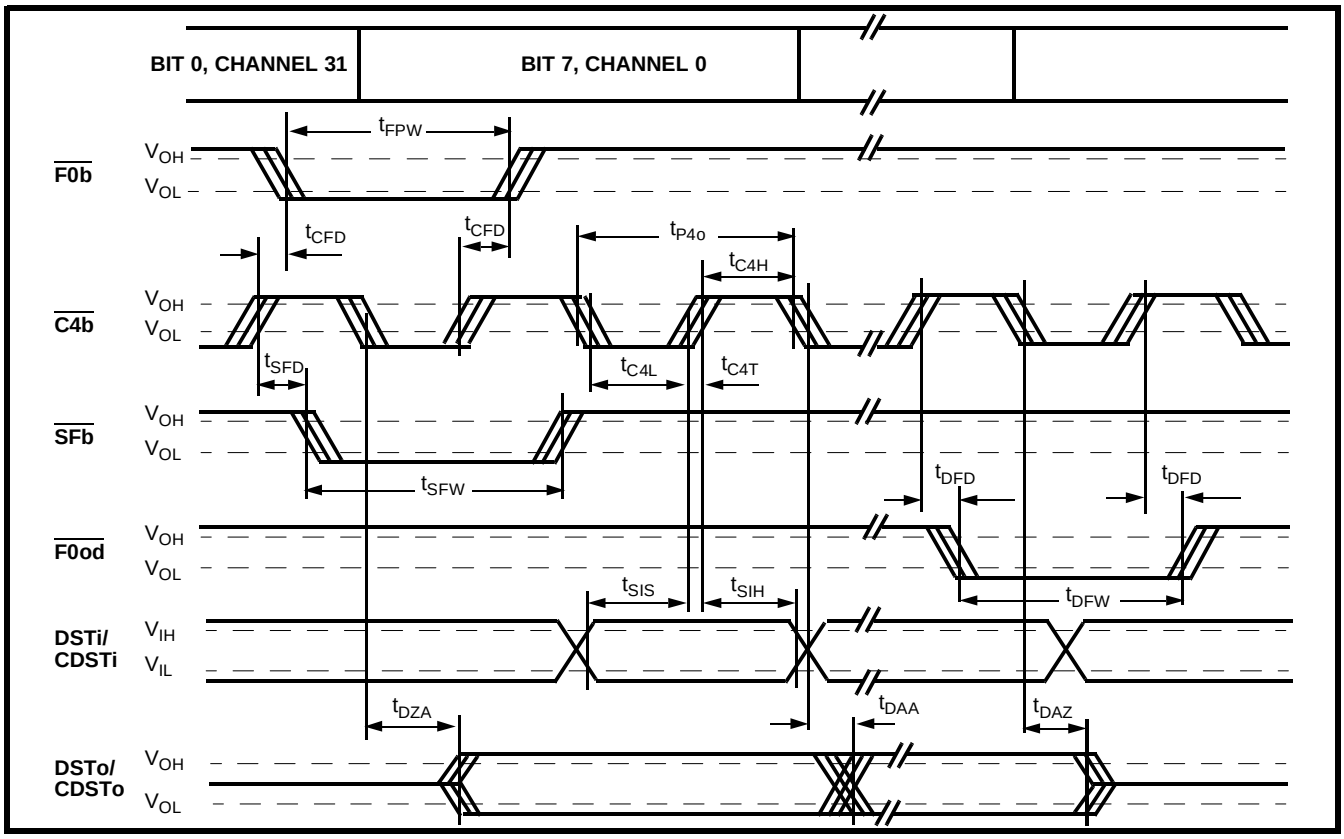


Figure 17 - ST-BUS Timing NT Mode

AC Electrical Characteristics† - ST-BUS Timing NT Mode (Ref. Figure 17)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{F0b}$ Output Pulse Width	t_{FPW}		1		cycles	C_L=150 pF, $\overline{C4b}$ cycles
2	$\overline{F0b}$ Output Delay	t_{CFD}			60	ns	150 pF (see Note 3)
3	$\overline{C4b}$ Output Clock Period	t_{P40}		244		ns	150 pF
4	$\overline{C4b}$ Pulse Width High	t_{C4H}		88		ns	150 pF
5	$\overline{C4b}$ Pulse Width Low	t_{C4L}		137		ns	150 pF (see Note 1)
6	$\overline{C4b}$ Transition Time	t_{C4T}		15		ns	150 pF
7	$\overline{SFb}$ Output Delay	t_{SFD}			60	ns	C_L=150 pF (see Note 3)
8	$\overline{SFb}$ Output Pulse Width	t_{SFW}		1		cycles	C_L=150 pF, $\overline{C4b}$ cycles
9	$\overline{F0od}$ Delay	t_{DFD}			60	ns	C_L=150 pF (see Notes 2 & 3)
10	$\overline{F0od}$ Pulse Width	t_{DFW}		1		cycles	C_L=150 pF, $\overline{C4b}$ cycles (see Note 2)
11	Serial Input Setup Time	t_{SIS}	30			ns	C_L=150 pF (see Note 2)
12	Serial Input Hold Time	t_{SIH}	50			ns	C_L=150 pF (see Note 2)
13	Serial Output Delay Act to Act	t_{DAA}			120	ns	150 pF load (see Notes 2 & 3)
	High Z to Act	t_{DZA}			120	ns	150 pF load (see Notes 2 & 3)
	Act to High Z	t_{DAZ}			120	ns	150 pF load (see Notes 2 & 3)

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Notes 1) The $\overline{C4b}$ pulse width low will vary by ±48ns during a phase-correction cycle.
2) These timing parameters are mode independent (NT or LT).
3) Tested at 5.0V, 25°C only.

NOTES: