

ADM9511

LAN/Modem Controller
with Embedded Fast Ethernet PHY

Revision 1.1 Jun. 2001

All Specifications subject to be changed without notice

ADMtek Inc. <http://www.admtek.com.tw>

ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY**

Revision History

| Release Date | Revision | Description |
|--------------------------|-----------------|---|
| October 2000 | 0.1 | Draft product spec for review |
| February 2001 | 1.0 | Add appendix 1 layout guide and format arrangement |
| June 2001 | 1.1 | Rename registers of CSR16, CSR17...etc. |

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ADM 9511
LAN/Modem Controller with Embedded Fast Ethernet PHY

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1. General Description

The ADM9511 is an Ethernet/Modem/HomePNA multifunction controller. It is the 2nd generation chipset of Centaur-P/C (AN983/985). In addition to all of the original Ethernet functions in Centaur, ADM9511 integrates the PCtel's host signal processing (HSP) modem interface in the chip to connect to PCtel's host signal processing modem data access arrangement (DAA) chipset.

On the LAN side, the ADM9511's fast Ethernet functions are fully compatible with Centaur. The system design can use the same software design as they did in Centaur with painlessness. On the system bus, the ADM9511 provides a glueless 32-bit PCI/CardBus bus master interface to connect to PCI/mini-PCI/Cardbus. On networking side, the ADM9511 integrates a fast Ethernet MAC controller with CSMA/CD protocol, as well as fast Ethernet PHY for 10BASE-T and 100BASE-TX. The auto-negotiation function is also supported for speed and duplex detection.

To provide modem solution, The ADM9511 provides te PCtel HSP modem interface, allow the system to provide PCtel's software modem solution.

To provide the HomePNA solution, the ADM9511 can be programmed as MAC-only controller, and provides the standard IEEE802.3 MII interface to connect to an external PHY. With the MII interface, it can connect to a wide range of 1M or 10M HomePNA MII PHY to provide the home networking solution.

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2. Features

Industry standard

- ⇒ Integrated IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant PHY
- ⇒ Support for IEEE802.3x flow control
- ⇒ IEEE802.3u Auto-Negotiation support
- ⇒ Glueless PCI/CardBus bus master interface
- ⇒ ACPI and PCI power management standards compliant
- ⇒ Support PC99 wake on LAN

FIFO

- ⇒ Provides two independent long FIFOs with 2k bytes each for transmit and receive
- ⇒ Pre-fetch up to two transmit packets to minimize inter frame gap(IFG) to 0.96us
- ⇒ Retransmits collided packet without reload from host memory within 64 bytes.
- ⇒ Automatically retransmits FIFO under-run packet with maximum drain threshold until 3 times retry failure and that will not influence the registers and transmit threshold of next packet

MAC/Physical

- ⇒ Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T
- ⇒ Provides an operation mode to isolate its internal PHY, use the standard IEEE802.3 MII interface to connect to an external PHY. With this mode, ADM9511 can support the HomePNA networking solution.
- ⇒ Provides Full -duplex operation on both 100Mbps and 10Mbps modes
- ⇒ Provides Auto-negotiation(NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- ⇒ Provides transmit wave-shaper, receive filters, and adaptive equalizer
- ⇒ Provides MLT-3 transceiver with DC restoration for Base-line wander compensation
- ⇒ Provides MAC and Transceiver(TXCVR) loop-back modes for diagnostic
- ⇒ Builds in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- ⇒ Supports external transmit transformer with turn ratio 1:1

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- ⇒ Supports external receive transformer with turn ratio 1:1

PCI/Cardbus I/F

- ⇒ Provides 32-bit PCI/Cardbus bus master data transfer
- ⇒ Supports system bus clock with frequency from 0Hz to 33MHz
- ⇒ Supports network operation with PCI/CardBus system clock from 20MHz to 33MHz
- ⇒ Provides performance meter, PCI/Cardbus bus master latency timer, for tuning the threshold to enhance the performance
- ⇒ Provides burst transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization
- ⇒ Supports memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master
- ⇒ Supports big or little endian byte ordering

EEPROM/Boot ROM I/F

- ⇒ Provides write-able Flash ROM and EPROM as boot ROM with size up to 128kB
- ⇒ Provides PCI/Cardbus to access boot ROM by byte, word, or double word
- ⇒ Re-writes Flash boot ROM through I/O port by programming register
- ⇒ Provides serial interface for read/write 93C66 EEPROM
- ⇒ Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency, and Minimum-Grand from the 64 byte contents of 93C66 after power-on reset.
- ⇒ CIS data is recalled from 93C66 to ADM9511 internal SRAM to speed up CIS access in CardBus environment.

Modem I/F

- ⇒ Provides the PCTel Host Signal Processing (HSP) modem interface, it allows the system to include PCTel' HSP modem solution to provide a LAN/Modem combo in PCI, CardBus, and Mini-PCI designs

LED Display

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- ⇒ (1) 3-LED display scheme provides:
 - ◆ 100Mbps(on) or Speed 10(off)
 - ◆ Link(keeps on when link ok) or Activity(will be blinking with 10Hz when receiving or transmitting but not collision)
 - ◆ FD(keeps on when in Full duplex mode) or Collision(will be blinking with 20Hz when colliding)
- (2) 4-LED display scheme provides:
 - ◆ 100Mbps and Link (keep on when link and 100Mbps)
 - ◆ 10Mbps and Link (keep on when link and 10Mbps)
 - ◆ Activity(will be blinking with 10Hz when receiving or transmitting but not collision)
 - ◆ FD(keeps on when in Full duplex mode) or Collision(will be blinking with 20Hz when colliding)

Miscellaneous

- ⇒ Provides 176-pin LPGA package
- ⇒ 3.3V power supply with 5V/3.3V I/O tolerance

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3. Typical Application

The ADM9511 supports Ethernet/Modem/HomePNA combination solution. On Ethernet application, it is a single chip with integrating Ethernet MAC controller and 10/100M Ethernet PHY, provides a glueless interface to system bus and network side. On modem application, the ADM9511 provides the PCtel HSP modem interface to connect to the PCtel HSP modem DAA chipsets. On HomePNA application, the ADM9511 provides a standard IEEE802.3 MII interface to connect to an external HomePNA PHY.

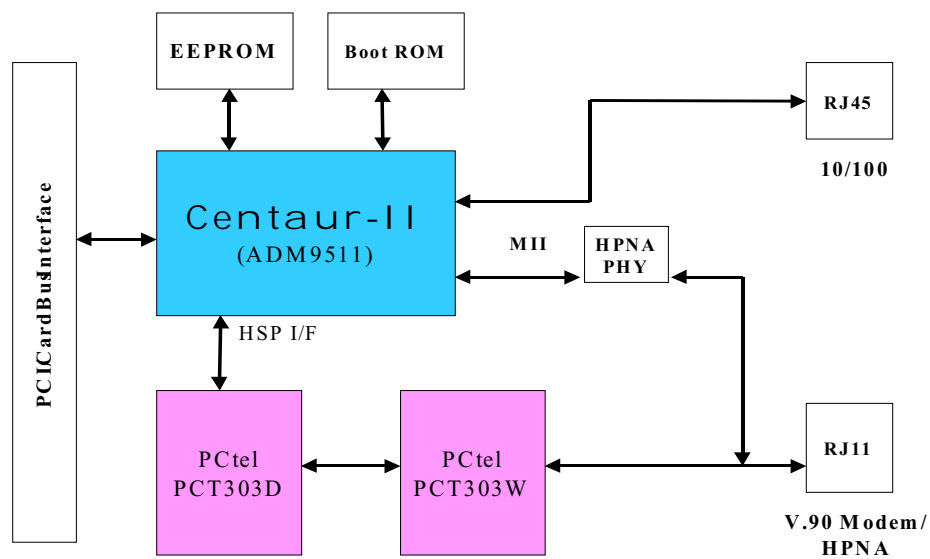


Figure 1 Typical Application

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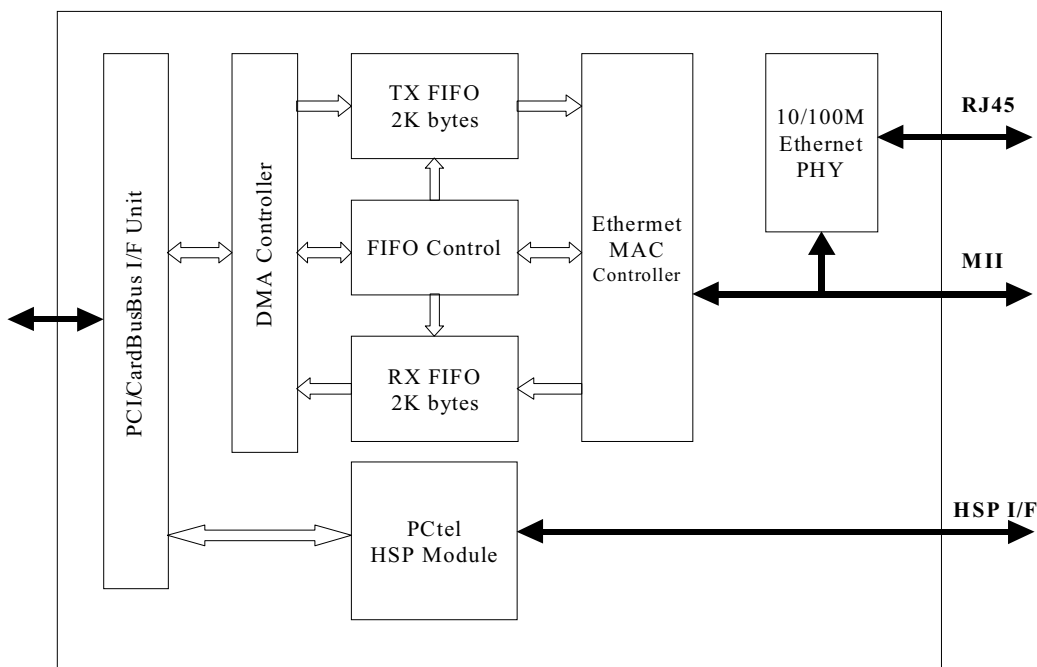
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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****4. Architecture Diagram****Figure 2 ADM9511 Architectural Block Diagram****ADMtek Inc.**

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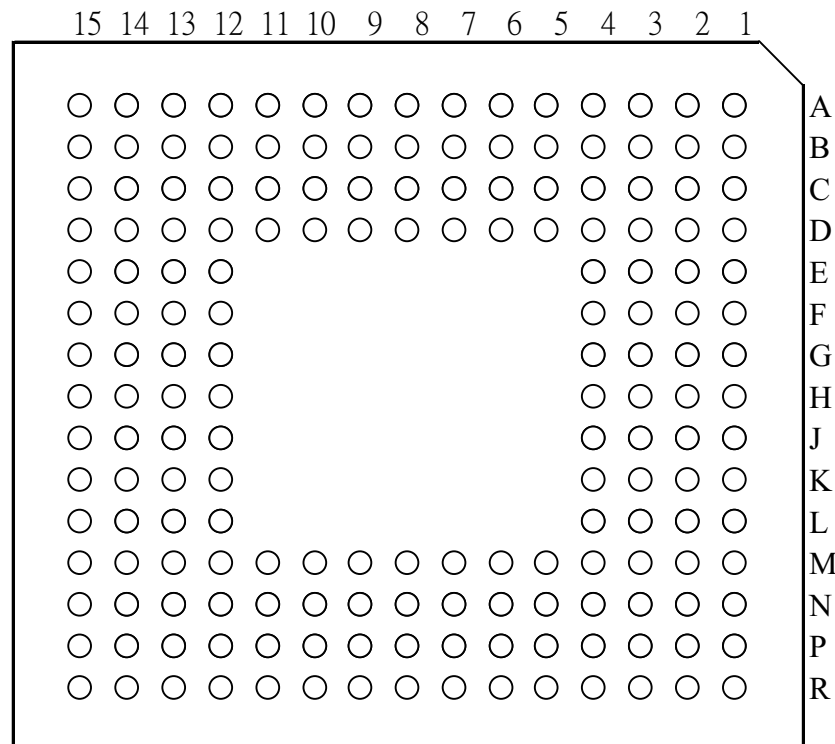
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5. Ball Grid Array Pin Out Diagram

The ADM9511 is a 176-pin LPGA package, the pinout diagram are shown in the following figure.



BOTTOM VIEW

Figure 3 ADM9511 176-pin LPGA pin out diagram

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****6. Pin Assignments**

| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---------|---------------|---------|-------------|---------|--------------|---------|-------|
| A1 | NC | C15 | BrOE# | H12 | BrA1 | N2 | AD25 |
| A2 | NC | D1 | RXIP | H13 | BrA2 | N3 | AD27 |
| A3 | MDIO | D2 | TST2 | H14 | VDD | N4 | AD21 |
| A4 | MDC | D3 | GNDR | H15 | LED-3 | N5 | AD18 |
| A5 | RXD2 | D4 | RXD0 | J1 | REQ# | N6 | VDD |
| A6 | RX_DV | D5 | RX_ER | J2 | PCI_CLK | N7 | VSS |
| A7 | VDD | D6 | TXD0 | J3 | VAAR | N8 | STOP# |
| A8 | TXD2 | D7 | COL | J4 | INTA# | N9 | PERR# |
| A9 | RING | D8 | BrA13 | J12 | AD0 | N10 | PAR |
| A10 | VDD | D9 | AFEMCLK | J13 | BrA0 | N11 | VSS |
| A11 | BrCS# | D10 | VSS | J14 | PMEP | N12 | AD11 |
| A12 | BrD6/EDI | D11 | EECS | J15 | Vdd_5V_3V | N13 | AD8 |
| A13 | BrD4 | D12 | BrA5 | K1 | AD29 | N14 | CBEZ0 |
| A14 | BrD3 | D13 | XTLM1 | K2 | PME#/CSTSCHG | N15 | NC |
| A15 | BrD1 | D14 | BrA8/ISPCI | K3 | RST# | P1 | AD24 |
| B1 | TST3 | D15 | BrA9/Vaux | K4 | VDD | P2 | CBEZ3 |
| B2 | VAAR | E1 | TST1 | K12 | AD2 | P3 | AD22 |
| B3 | NC | E2 | GNDR | K13 | AD1 | P4 | VSS |
| B4 | RXD3 | E3 | NC | K14 | Vcc_detect | P5 | AD16 |
| B5 | RX_CLK | E4 | TST0 | K15 | CLKRUN | P6 | IRDY# |
| B6 | TX_CLK | E12 | XTLM2 | L1 | VDD | P7 | VDD |
| B7 | TXD1 | E13 | GPIO2 | L2 | AD30 | P8 | SERR# |
| B8 | CRS | E14 | VSS | L3 | GNT# | P9 | VSS |
| B9 | BrA14 | E15 | BrA7 | L4 | AD31 | P10 | AD13 |
| B10 | BrA11/OFF_HK | F1 | RIBB | L12 | AD5 | P11 | VDD |
| B11 | SCLK | F2 | XTLP | L13 | AD3 | P12 | NC |
| B12 | SDI | F3 | VAAR | L14 | VSS | P13 | VSS |
| B13 | BrD5/EDO | F4 | NC | L15 | VDD | P14 | NC |
| B14 | BrD2 | F12 | GPIO1 | M1 | NC | P15 | NC |
| B15 | BrD0 | F13 | LED-2 | M2 | AD26 | R1 | VSS |
| C1 | RXIN | F14 | VDD | M3 | VSS | R2 | IDSEL |
| C2 | NC | F15 | VSS | M4 | AD28 | R3 | AD23 |
| C3 | RXD1 | G1 | GNDR | M5 | AD20 | R4 | VDD |
| C4 | VSS | G2 | NC | M6 | AD17 | R5 | AD19 |
| C5 | TX_EN | G3 | TXOP | M7 | FRAME# | R6 | CBEZ2 |
| C6 | TXD3 | G4 | XTLN | M8 | DEVSEL# | R7 | TRDY# |
| C7 | NC | G12 | LED-1 | M9 | VDD | R8 | CBEZ1 |
| C8 | BrA15 | G13 | BrA3 | M10 | AD15 | R9 | AD14 |
| C9 | BrA12/AFERST# | G14 | BrA16/LED-4 | M11 | AD12 | R10 | AD10 |

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| | | | | | | | |
|-----|-----------|-----|------|-----|-----|-----|-----|
| C10 | FS | G15 | BrA4 | M12 | AD9 | R11 | NC |
| C11 | BrA10/SDO | H1 | VSS | M13 | AD6 | R12 | NC |
| C12 | BrD7/ECK | H2 | VDD | M14 | AD4 | R13 | NC |
| C13 | BrA6 | H3 | TXON | M15 | AD7 | R14 | VSS |
| C14 | BrWE# | H4 | NC | N1 | NC | R15 | NC |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****7. Pin Description**

| Name | Type | Description |
|------------------------|------------|---|
| ● PCI Interface | | |
| INTA# | O/D | PCI interrupt request. ADM9511 asserts this signal when one of the interrupts occurred. |
| RST# | I | PCI signal to initialize the ADM9511. The active reset signal should be sustained at least 100 μ s to guarantee that the ADM9511 has completed the initializing activity. During the reset period, all the output pins of ADM9511 will be set to tri-state and all the O/D pins are floated. |
| PCI_CLK | I | This PCI clock inputs to ADM9511 for PCI relative circuits as the synchronized timing base with PCI bus. The Bus signals are recognized on rising edge of PCI_CLK. In order to let network operating properly, the frequency range of PCI_CLK is limited between 20MHz and 33MHz when network operating. |
| GNT# | I | PCI Bus Granted. This signal indicates that the bus request of ADM9511 have been accepted. |
| REQ# | O | PCI Bus Request. Bus master device want to get bus access right |
| PME# / CSTSCHG | I/O | The Power Management Event signal is an open drain, active low signal for PCI (PME#), active high for CardBus (CSTSCHG). When bit 18 of CSR18 is set into "1", means that the ADM9511 is set into Wake On LAN mode. In this mode, when the ADM9511 receives a Magic Packet frame from network then the ADM9511 will active this signal too. |
| AD0-AD31 | I/O | Multiplexed address data pin of PCI Bus |
| CBEZ0- CBEZ3 | I/O | Bus command and byte enable |
| IDSEL | I | Initialization Device Select. This signal is asserted when host issues the configuration cycles to the ADM9511. |
| FRAME# | I/O | Begin and duration of bus access, driven by master device |
| IRDY# | I/O | Master device is ready to data transaction |
| TRDY# | I/O | Slave device is ready to data transaction |
| DEVSEL# | I/O | Device select, target is driving to indicate the address is decoded |
| STOP# | I/O | Target device request the master device to stop the current transaction |
| PERR# | I/O | Data parity error is detected, driven by the agent receiving data |
| SERR# | O/D | Address parity error |
| PAR | I/O | Parity, even parity (AD[31:0] + CBE[3:0]), master drives par for address and write data phase, target drives par for read data phase |
| CLKRUN | I/O O/D | Clock Run for PCI system. In the normal operation situation, Host should assert this signal to indicate ADM9511 about the normal situation. On the other hand, when Host will de-assert this signal when the clock is going down to a non-operating frequency. When ADM9511 recognizes the de-asserted status of CLKRUN, then it will assert CLKRUN to request host to maintain the normal clock operation. When CLKRUN function is disabled then the ADM9511 will set CLKRUN in tri-state. |

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| ● BootROM/EEPROM Interface | | |
|-----------------------------------|---------|---|
| BrA0 -BrA16 | I/O | ROM data bus Provides up to 128kB EPROM or Flash-ROM application space. |
| BrD0-BrD4 | O | BootROM data bus bit (0~7) |
| BrD5/EDO | O/I | EDO: Data Output of serial EEPROM, Inputs data to ADM9511 |
| BrD6/EDI | O/O | EDI: Data Input of serial EEPROM, the ADM9511 outputs data to EEPROM |
| BrD7/ECK | O/O | ECK: Clock input of serial EEPROM, the ADM9511 outputs clock signal to EEPROM |
| EECS | O | Chip Select of serial EEPROM |
| BrCS# | O | BootROM Chip Select |
| BrOE# | O | BootROM Read Enable for flash ROM application |
| BrWE# | O | BootROM Write Enable for flash ROM application. |
| ● Software Modem Interface | | |
| AFERST# | O | AFE reset output for external CODEC. This pin is used as the AFE reset signal for external CODEC. |
| OFF_HK | O | Off_hook relay control output. This pin is used as the active-high control for the OFFHOOK Relay. It is driven by bit 0 of the modem external output register |
| RING | I | Ring detection input. It is used to indicate that the telephone ring is detected. The RING signal can be red through bit 0 of the modem external input register. |
| FS | I | Frame synchronization input. This signal is driven by external CODEC to indicate that the device is ready to send and receive data. The data transfer begins on the rising edge of SCLK. |
| SCLK | I | Serial clock input. The serial clock is driven by external CODEC as the reference clock for serial data communication between external CODEC and the ADM9511 |
| SDI | I | Serial data input from external CODEC. The serial data input is the path for serial bit stream driving from the CODEC to the ADM9511. The serial input data is sampled on the falling edge of SCLK. |
| SDO | O | Serail data output to external CODEC. The serial data output is the path for serial bit stream driving from the ADM9511 to the CODEC. The serial output data is clocked by the rising edge of SCLK. |
| AFEMCLK | O | Master clock to external CODEC. This is a programmable clock output which is provided as the master clock input for the external CODEC. |
| XTLM2, XTLM1 | O, I | Terminals to connect to external crystal. The recommended frequency of the quartz crystal for software modem is 18.432 MHZ +- 50ppm frequency tolerance at room temperature |
| GPIO1, GPIO2 | I/O | General purpose pins |
| MII Interface | | |
| RXD0-RXD 3 | I | MII Receive data |
| CRS | I | MII carrier sense |
| COL | I | MII collision detection |
| RX_ER | I | MII Receive data error |
| RX_DV | I | MII Receive data valid |
| TX_EN | O | MII Transmit enable |
| TXD0-TXD | O | MII Transmit data |

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| | | |
|--|-----|--|
| 3 | | |
| TX_CLK | I | MII Transmit clock |
| RX_CLK | I | MII Receive clock |
| MDC | O | MII Management data control |
| MDIO | I/O | MII Management data in/out |
| ● Physical Interface | | |
| XTLN, XTLP | I | Crystal inputs. To be connected to a 25MHz crystal. |
| RXIN, RXIP | I | The differential receive inputs of 100BASE-TX or 10BASE-T, these pins directly input from Magnetic. |
| TXOP, TXON | O | The differential Transmit outputs of 100BASE-TX or 10BASE-T, these pins directly output to Magnetic. |
| RIBB | I | Reference Bias Resistor. To be tied to an external 10.0K (1%) resistor which should be connected to the analog ground at the other end. |
| TST0-TST3 | I | Test pins |
| ● LED display and Miscellaneous | | |
| LED-1 | O | There is an internal pull-up resistor 30k. Led-Act (Led-lk/act): 4Leds mode: LED display for Activity status. This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. (3Led mode): LED display for link and activity status. This pin will be driven on continually when a good Link test is detected. This pin will be driven on with 10 Hz blinking frequency when either effective receiving or transmitting is detected. |
| LED-2 | O | There is an internal pull-up resistor 30k. Led-10Lnk (Led-fd/col): 4Leds mode: LED display for 10M b/s speed. This pin will be driven on continually when the 10M b/s network operating speed is detected. (3Leds mode): LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. |
| LED-3 | O | There is an internal pull-up resistor 30k. Led-100Lnk (Led-speed): 4Leds mode: LED display for 100Mb/s speed. This pin will be driven on continually |

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| | | |
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| | | when the 100Mb/s network operating speed is detected. (3Leds mode): LED display for 100M b/s or 10M b/s speed. This pin will be driven on continually when the 100M b/s network operating speed is detected. |
| LED-4 | O | There is an internal pull-up resistor 30k. Led-Fd/Col (None) 4Leds mode: LED display for Full Duplex or Collision status. This pin will be driven on continually when a full duplex configuration is detected. This pin will be driven on with 20 Hz blinking frequency when a collision status is detected in the half duplex configuration. (3Leds mode): None |
| Vaux | I | Reset latched signal , multiplex with BrA9 This pin should be pull-up by resistor 4.7k When this pin is asserted, it indicates an auxiliary power source is supported ACPI purpose , for detecting the auxiliary power source . This pin should be or-wired connected to 1) 3.3V when 3.3Vaux support , or 2) 5V when 5Vaux support from 3-way switch. |
| Vcc_detect | I | When this pin is asserted, it indicates PCI power source is supported. ACPI purpose , for detecting the main power is remained or not , this pin should be connected by a resistor 680 ohm to PCI bus power source +5V. |
| Vdd_5V_3V | I(A) | Analogue input pin voltage referenced level for 3v/5v tolerance i/o cell. The voltage of this pin depends on what kind of bus(PCI or Cardbus.) connected. i.e. PCI (5V) 1) 5V when main power exists or 2) 3.3V when 3.3Vaux support (PCI 2.2 , D3cold , no 5V power source) , or 3) 5V when 5Vaux support from 3-way switch. (D3cold mode) |
| ISPCI | I | Reset latched signal , multiplex with BrA8 1: Put ADM9511 on PCI mode; pull-up a resistor 4.7k to +3.3V 0 :Put ADM9511 on Cardbus mode; pull-down a resistor 4.7k to ground |
| PMEP | O | This signal is used as the WOL pin. It provided a programmable positive or negative pulse with approximately 50ms width. |
| ● Digital Power Pins | | |
| VDD | | Digital power supply, connect to +3.3V |
| VSS | | Digital ground |
| ● Analog Power Pins | | |
| VAAR | | Analog power supply, connect to +3.3V |
| GNDR | | Analog ground |

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8. Registers and Descriptors Description

8.1.PCI/CardBus Configuration Registers

8.1.1. Function 0: Ethernet PCI Configuration Registers

With the configuration registers, software driver can initialize and configure ADM9511. All of the contents of configuration registers are set to default value when there is any hardware reset occurs. On the other hand, there is no effect to their value when the software reset occurs. To access these configuration registers ADM9511 provides byte, word, and double word data access length.

8.1.1.1. Ethernet PCI configuration registers list

| Offset | Index | Name | Descriptions |
|--------|-------|------|--|
| 00h | CR0 | LID | Loaded device ID and vendor ID |
| 04h | CR1 | CSC | Configuration Status and Command |
| 08h | CR2 | CC | Class Code and revision number |
| 0ch | CR3 | LT | Latency Timer |
| 10h | CR4 | IOBA | IO Base Address |
| 14h | CR5 | MBA | Memory Base Address |
| 28h | CR10 | CIS | Card Information Structure(for Card bus) |
| 2ch | CR11 | SID | Subsystem ID and vendor ID |
| 30h | CR12 | BRBA | Boot ROM Base Address (ROM size = 128KB) |
| 34h | CR13 | CP | Capability Pointer |
| 3ch | CR15 | CINT | Configuration Interrupt |
| 40h | CR16 | DS | driver space for special purpose |
| 80h | CR32 | SIG | Signature of ADM9511 |
| c0h | CR48 | PMR0 | Power Management Register 0 |
| c4h | CR49 | PMR1 | Power Management Register 1 |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****8.1.1.2. Ethernet PCI configuration registers table**

| Offset | b31 | ----- | b16 | b15 | ----- | b0 |
|-------------|-----------------------|-----------------------|----------|----------------------|-----------------|--------|
| 00h | Device ID* | | | Vendor ID* | | |
| 04h | Status | | | Command | | |
| 08h | Base Class Code | | Subclass | ---- | Revision # | Step # |
| 0ch | ----- | Header Type | | Latency Timer | Cache Line Size | |
| 10h | Base I/O address | | | | | |
| 14h | Base memory address | | | | | |
| 18h~ 24h | Reserved | | | | | |
| 28h | ROM-im* | Address space offset* | | | Add-indi* | |
| 2ch | Subsystem ID* | | | Subsystem vendor ID* | | |
| 30h | Boot ROM base address | | | | | |
| 34h | Reserved | | | | Cap_Ptr | |
| 38h | Reserved | | | | | |
| 3ch | Max_Lat* | | Min_Gnt* | Interrupt pin | Interrupt line | |
| 40h | Reserved | | | Driver Space | Reserved | |
| 80h | Signature of ADM9511 | | | | | |
| c0h | PMC | | | Next_Item_Ptr | Cap_ID | |
| c4h | ----- | Data register | | PMCSR | | |

Note: * : automatically recalled from EEPROM when PCI reset is deserted

CIS(28h) is a read-only register

DS(40h), bit15-8 is read/write able register

SIG(80h) is hard wired register, read only.

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****8.1.1.3. Ethernet PCI configuration registers description****CR0 (offset = 00h), LID - Loaded Identification number of Device and Vendor**

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | LDID | Loaded Device ID, the device ID number loaded from serial EEPROM. | From EEPROM | R/O |
| 15~0 | LVID | Loaded Vendor ID, the vendor ID number loaded from serial EEPROM. | From EEPROM | R/O |

From EEPROM: Loaded from EEPROM

CR1 (offset = 04h), CSC - Configuration command and status

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|---|-------------------|---------|
| 31 | SPE | Status of Parity Error. 1: means that ADM9511 detected a parity error. This bit will be set in this condition, even if the parity error response (bit 6 of CR1) is disabled. | 0 | R/W |
| 30 | SES | Status of System Error. 1: means that ADM9511 asserted the system error pin. | 0 | R/W |
| 29 | SMA | Status of Master Abort. 1: means that ADM9511 received a master abort and terminated a master transaction. | 0 | R/W |
| 28 | STA | Status of Target Abort. 1: means that ADM9511 received a target abort and terminated a master transaction. | 0 | R/W |
| 27 | --- | Reserved | | |
| 26, 25 | SDST | Status of Device Select Timing. The timing of the assertion of device select. 01: means a medium assertion of DEVSEL# | 01 | R/O |
| 24 | SDPR | Status of Data Parity Report. 1: when three conditions are met: a. ADM9511 asserted parity error - PERR# or it detected parity error asserted by other device. b. ADM9511 is operating as a bus master. c. ADM9511's parity error response bit (bit 6 of CR1) is enabled. | 0 | R/W |
| 23 | SFBB | Status of Fast Back-to-Back Always 1, since ADM9511 has the ability to accept fast back to back transactions. | 1 | R/O |
| 22~21 | --- | Reserved | | |
| 20 | NC | New Capabilities. This bit indicates that whether the ADM9511 provides a list of extended capabilities, such as | Same as bit 19 of | RO |

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|-------|-------|---|-------|-----|
| | | PCI power management. 1: the ADM9511 provides the PCI management function 0: the ADM9511 doesn't provide New Capabilities. | CSR18 | |
| 19~ 9 | --- | Reserved | | |
| 8 | CSE | Command of System Error Response 1: enable system error response. ADM9511 will assert SERR# when it finds a parity error on the address phase. | 0 | R/W |
| 7 | --- | Reserved | | |
| 6 | CPE | Command of Parity Error Response 0: disable parity error response. ADM9511 will ignore any detected parity error and keep on its operating. Default value is 0. 1: enable parity error response. ADM9511 will assert system error (bit 13 of CSR5) when a parity error is detected. | 0 | R/W |
| 5~ 3 | --- | Reserved | | |
| 2 | CMO | Command of Master Operation Ability 0: disable the bus master ability. 1: enable the PCI bus master ability. Default value is 1 for normal operation. | 0 | R/W |
| 1 | CMSA | Command of Memory Space Access 0: disable the memory space access ability. 1: enable the memory space access ability. | 0 | R/W |
| 0 | CIOSA | Command of I/O Space Access 0: enable the I/O space access ability. 1: disable the I/O space access ability. | 0 | R/W |

R/W: Read and Write able. RO: Read able only.

CR2 (offset = 08h), CC - Class Code and Revision Number

| Bit # | Name | Descriptions | Default Val | R/W Type |
|-------|------|--|-------------|----------|
| 31~24 | BCC | Base Class Code. It means ADM9511 is network controller. | 02h | RO |
| 23~16 | SC | Subclass Code. It means ADM9511 is a Fast Ethernet Controller. | 00h | RO |
| 15~ 8 | --- | Reserved | | |
| 7 ~ 4 | RN | Revision Number, identifies the revision number of ADM9511. | TBD | RO |
| 3 ~ 0 | SN | Step Number, identifies the ADM9511 steps within the current revision. | TBD | RO |

RO: Read Only.

CR3 (offset = 0ch), LT - Latency Timer

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| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~24 | ---- | Reserved | | |
| 23~16 | HT | The value is depended on the modem enable/disable status that read from EEPROM. If modem function is enabled, the HT value is 80h, else, the HT value is 00h. A value of 80h to indicate ADM9511 is a multiple function device for a combination of Ethernet and modem card. The OS will read the modem configuration registers at offset 100h | From EEPROM | RO |
| 15~ 8 | LT | Latency Timer. This value specifies the latency timer of the ADM9511 in units of PCI bus clock. Once the device asserts FRAME#, the latency timer starts to count. If the latency timer expires and the device still asserted FRAME#, then the device will terminate the data transaction as soon as its GNT# is removed. | 0 | R/W |
| 7 ~ 0 | CLS | Cache Line Size. This value specifies the system cache line size in units of 32-bit double words (DW). The ADM9511 supports 8, 16, and 32 DW of cache line size. This value is used by the ADM9511 driver to program the cache alignment bits(bit 14 and 15 of CSR0). The cache alignment bits are used for cache oriented PCI commands, say memory-read-line, memory-read-multiple, and memory-write-and-invalidate. | 0 | R/W |

CR4 (offset = 10h), IOBA - I/O Base Address

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~ 8 | IOBA | I/O Base Address. This value indicate the base address of PCI control and status register(CSR0~34) | 0 | R/W |
| 7 ~ 1 | --- | Reserved | | |
| 0 | IOSI | I/O Space Indicator. 1: means that the configuration registers map into the I/O space. | 1 | RO |

CR5 (offset = 14h), MBA - Memory Base Address

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|--|-------------|---------|
| 31~ 10 | MBA | Memory Base Address. This value indicate the base address of PCI control and status register (CSR0~34) | 0 | R/W |

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| | | | | |
|-------|------|---|---|----|
| 9 ~ 1 | --- | Reserved | | |
| 0 | IOSI | Memory Space Indicator. 0: means that the configuration registers map into the memory space. | 0 | RO |

CR10 (offset = 28h), CIS - Card Information Structure

This register is used to point one of the possible address spaces where the CIS begins. This register is designed for PCI environment. It's data is auto-loaded from the serial EEPROM after power on or hardware reset.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~28 | RI | ROM Image. This ROM image value is applied when the CIS is stored in a boot ROM. This value is loaded from serial EEPROM. | From EEPROM | RO |
| 27~ 3 | ASO | Address Space Offset. This value indicates the offset within the address space. The address space is specified by address space indicator(bit 2~0 of CR10). | From EEPROM | RO |
| 2 ~ 0 | ASI | Address Space Indicator. This value indicates the location where the CIS address space begins. 7: means that the CIS begins in the boot ROM space. Other than 7: makes all the bits of CIS reset to 0. | From EEPROM | RO |

CR11 (offset = 2ch), SID - Subsystem ID.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | SID | Subsystem ID. This value is loaded from EEPROM after power on or hardware reset. | From EEPROM | RO |
| 15~ 0 | SVID | Subsystem Vendor ID. This value is loaded from EEPROM after power on or hardware reset. | From EEPROM | RO |

CR12 (offset = 30h), BRBA - Boot ROM Base Address.

This register should be initialized before accessing the boot ROM space. (write 32'hffffff return 32'h fffe0001)

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|------------------------|---------|
| 31~17 | BRBA | Boot ROM Base Address. This value indicates the address mapping of boot ROM field. Besides, it also defines the boot ROM size. The value of bit 17~10 is set to 0 for ADM9511 supports up to 128kB of boot ROM. | X: b31~18 0: b17~10 | R/W |

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| | | | | |
|--------|-----|---|---------------------|-----|
| 16 ~ 1 | --- | Reserved | 0 | |
| 0 | BRE | <p>Boot ROM Enable. The ADM9511 really enables its boot ROM access only if both the memory space access bit(bit 1 of CR1) and this bit are set to 1.</p> <p>1: enable Boot ROM. (Combines with bit 1 of CR1)</p> <p>0: disable Boot ROM.</p> <p>After Boot ROM is accessed completely, this bit should be reset to enable modem interface</p> | 0 from eeprom | R/W |

CR13 (offset = 34h), CP - Capabilities Pointer.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|-----------------------|-------------|---------|
| 31~8 | --- | Reserved | | |
| 7~0 | CP | Capabilities Pointer. | C0h | RO |

CR15 (offset = 3ch), CINT - Configuration Interrupt

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|----------------|---------|
| 31~24 | ML | Max_Lat register. This value indicates “how often” the ADM9511 needs to access to the PCI bus in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset. | From EEPROM | RO |
| 23~16 | MG | Min_Gnt register. This value indicates “how long” the ADM9511 needs to retain the PCI bus ownership whenever it initiates a transaction in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset. | From EEPROM | RO |
| 15~ 8 | IP | Interrupt Pin. This value indicates which of the four interrupt request pins that ADM9511 is connected. Always 01h: means the ADM9511 connects to INTA# | 01h | RO |
| 7 ~ 0 | IL | Interrupt Line. This value indicates which of the system interrupt request lines the INTA# of ADM9511 is routed to. The BIOS will fill this field when it initializes and configures the system. The ADM9511 driver can use this value to determine priority and vector information. | X | R/W |

CR16 (offset = 40h), DS - Driver Space for special purpose.**ADMtek Inc.**

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| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | --- | reserved | | |
| 15~8 | DS | Driver Space for special purpose. Since this area won't be cleared in the software reset. The ADM9511 driver can use this R/W area for special purpose. | X | R/W |
| 7~0 | --- | Reserved | | |

CR32 (offset = 80h), SIG - Signature of ADM9511

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | DID | Device ID, the device ID number of ADM9511. | 6985h | RO |
| 15~0 | VID | Vendor ID, the vendor ID number of ADM Technology Corp. | 1317h | RO |

CR48 (offset = c0h), PMR0, Power Management Register0.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~27 | PMES | PME_Support. The ADM9511 will assert PME#/CSTSCHG signal while in the D0, D1, D2, D3hot power state. The ADM9511 supports Wake-up from the above four states. | 11111b | RO |
| 26 | D2S | D2_Support. The ADM9511 supports D2 Power Management State. | 1 | RO |
| 25 | D1S | D1_Support. The ADM9511 supports D1 Power Management State. | 1 | RO |
| 24~22 | AUXC | Aux. Current. These three bits report the maximum 3.3 Vaux current requirements for ADM9511. If bit 31 of PMR0 is '1', the default value is 0101b, means ADM9511 need 100 mA to support remote wake-up in D3cold power state. | 010b | RO |
| 21 | DSI | The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. 0: indicates that the function does not require a device specific initialization sequence following transition to the D0 un-initialized state. | 0 | RO |
| 20 | --- | Reserved. | 0 | RO |
| 19 | PMEC | PME Clock. When "1" indicates that the ADM9511 relies on the presence of the PCI clock for PME#/CSTSCHG | 0 | RO |

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|-------|-------|---|------|----|
| | | operation. While “0” indicates the no PCI clock is required for the ADM9511 to generate PME#/CSTSCHG. | | |
| 18~16 | VER | Version. The value of 010b indicates that the ADM9511 complies with Revision 1.1 of the PCI Power Management Interface Specification. | 010b | RO |
| 15~8 | NIP | Next Item Pointer. This value is always 0h, indicates that there is no additional items in the Capabilities List. | 00h | RO |
| 7~0 | CAPID | Capability Identifier. This value is always 01h, indicates the link list item as being PCI Power Management Registers. | 01h | RO |

CR49 (offset = c4h), PMR1, Power Management Register 1.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|--------|---|-------------|---------|
| 31~24 | DR | Data register. This register is used to report the state dependent data requested by the data_select field. The value of this register is scaled by the value reported by the data_scale field | From EEPROM | RO |
| 23~16 | ----- | Reserved | 8'b0 | RO |
| 15 | PMES | PME_Status, This bit is set when the ADM9511 would normally assert the PME#/CSTSCHG signal for wake-up event, this bit is independent of the state of the PME-En bit. Writing a “1” to this bit will clear it and cause the ADM9511 to stop asserting a PME#/CSTSCHG (if enabled). Writing a “0” has no effect. | 0 | R/W* |
| 14,13 | DSCAL | Data_Scale, indicates the scaling factor to be used when interpreting the value of the Data register. | 0 | RO |
| 12~9 | DSEL | Data_Select, This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. | 0 | R/W |
| 8 | PME_En | PME_En, “1” enables the ADM9511 to assert PME#/CSTSCHG. When “0” disables the PME#/CSTSCHG assertion. Magic packet default enable: When CSR18<18> and CSR18<19> are set to 1, then the magic packet wake up event will be default enabled (CSR13<9> be set), it doesn't matter the PME_En is set or not. | 0 | R/W |
| 7~2 | --- | Reserved | 6'b000000 | RO |
| 1,0 | PWRS | Power State. This two-bit field is used both to determine the current power state of the ADM9511 and to set the ADM9511 into a new power state. The definition of this field is given below. 00b - D0 | 00b | R/W |

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| | | | | |
|--|--|--|--|--|
| | | 01b - D1 10b - D2 11b - D3hot This field is auto cleared to D0 when power resumed . | | |
|--|--|--|--|--|

R/W*: Read and Write clear

Ethernet data register :

| Data select | Data scale | Value | Data reported |
|-------------|------------|-------|----------------------------------|
| 0 | 2 | TBD | D0 power consumption |
| 1 | 2 | TBD | D1 power consumption |
| 2 | 2 | TBD | D2 power consumption |
| 3 | 2 | TBD | D3 power consumption |
| 4 | 2 | TBD | D0 power dissipated |
| 5 | 2 | TBD | D1 power dissipated |
| 6 | 2 | TBD | D2 power dissipated |
| 7 | 2 | TBD | D3 power dissipated |
| 8 | 2 | TBD | Common function power dissipated |
| 9-15 | 2 | TBD | Reserved |

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8.1.2. Function 1: Modem PCI Configuration Registers

The AD9511 supports a dual function device: LAN/Modem. The modem is defined as function 1. The modem configuration registers are located at offset 100h. With the configuration registers, software driver can initialize and configure ADM9511 modem function. All the contents of configuration registers are set to default values when there is any hardware reset occurs. On the other hand, there is no effect to their value when the software reset occurs. To access these configuration registers ADM9511 provides byte, word, and double word data access length.

8.1.2.1. Modem PCI configuration registers list

| Offset | Index | Name | Descriptions |
|---------------|--------------|-------------|--|
| 100h | MCR0 | LID | Loaded device ID and vendor ID |
| 104h | MCR1 | CSC | Configuration Status and Command |
| 108h | MCR2 | CC | Class Code and revision number |
| 10ch | MCR3 | LT | Latency Timer |
| 110h | MCR4 | IOBA | IO Base Address |
| 114h | MCR5 | MBA | Memory Base Address |
| 128h | MCR10 | CIS | Card Information Structure(for Card bus) |
| 12ch | MCR11 | SID | Subsystem ID and vendor ID |
| 130h | MCR12 | BRBA | Boot ROM Base Address |
| 134h | MCR13 | CP | Capability Pointer |
| 13ch | MCR15 | CINT | Configuration Interrupt |
| 140h | MCR16 | DS | driver space for special purpose |
| 180h | MCR32 | SIG | Signature of ADM9511 |
| 1c0h | MCR48 | PMR0 | Power Management Register 0 |
| 1c4h | MCR49 | PMR1 | Power Management Register 1 |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****8.1.2.2. Modem PCI configuration registers table**

| Offset | b31 | ----- | b16 | b15 | ----- | b0 |
|---------------|-----------------------|-----------------------|-----|----------------------|-----------------|--------|
| 100h | Device ID* | | | Vendor ID* | | |
| 104h | Status | | | Command | | |
| 108h | Base Class Code | Subclass | | PI | Revision # | Step # |
| 10ch | ----- | Header Type | | Latency Timer | Cache Line Size | |
| 110h | Base I/O address | | | | | |
| 114h | Base memory address | | | | | |
| 118h~ 124h | Reserved | | | | | |
| 128h | ROM-im* | Address space offset* | | | Add-indi* | |
| 12ch | Subsystem ID* | | | Subsystem vendor ID* | | |
| 130h | Boot ROM base address | | | | | |
| 134h | Reserved | | | | Cap_Ptr | |
| 138h | Reserved | | | | | |
| 13ch | Max_Lat* | Min_Gnt* | | Interrupt pin | Interrupt line | |
| 140h | Reserved | | | Driver Space | Reserved | |
| 180h | Signature of ADM9511 | | | | | |
| 1c0h | PMC | | | Next_Item_Ptr | Cap_ID | |
| 1c4h | ----- | Data register | | PMCSR | | |

Note: *: automatically recalled from EEPROM when PCI reset is deserted

CIS (128h) is a read-only register

DS (140h), bit15-8 is read/write able register

SIG (180h) is hard wired register, read only.

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****8.1.2.3. Modem PCI configuration registers description****MCR0 (offset = 100h), LID - Loaded Identification number of Device and Vendor**

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | DID | Loaded Device ID, the device ID number loaded from serial EEPROM. | From EEPROM | R/O |
| 15~0 | VID | Loaded Vendor ID, the vendor ID number loaded from serial EEPROM. | From EEPROM | R/O |

From EEPROM: Loaded from EEPROM

MCR1 (offset = 104h), CSC - Configuration command and status

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|---|-------------------|---------|
| 31 | SPE | Status of Parity Error. 1: means that ADM9511 detected a parity error. This bit will be set in this condition, even if the parity error response (bit 6 of MCR1) is disabled. | 0 | R/W |
| 30 | SES | Status of System Error. 1: means that ADM9511 asserted the system error pin. | 0 | R/W |
| 29 | SMA | Status of Master Abort. 1: means that ADM9511 received a master abort and terminated a master transaction. | 0 | R/W |
| 28 | STA | Status of Target Abort. 1: means that ADM9511 received a target abort and terminated a master transaction. | 0 | R/W |
| 27 | --- | Reserved | | |
| 26, 25 | SDST | Status of Device Select Timing. The timing of the assertion of device select. 01: means a medium assertion of DEVSEL# | 01 | R/O |
| 24 | SDPR | Status of Data Parity Report. 1: when three conditions are met: a. ADM9511 asserted parity error - PERR# or it detected parity error asserted by other device. b. ADM9511 is operating as a bus master. c. ADM9511's parity error response bit(bit 6 of MCR1) is enabled. | 0 | R/W |
| 23 | SFBB | Status of Fast Back-to-Back Always 1, since ADM9511 has the ability to accept fast back to back transactions. | 1 | R/O |
| 22~21 | --- | Reserved | | |
| 20 | NC | New Capabilities. This bit indicates that whether the ADM9511 provides a list of extended capabilities, such as | Same as bit 19 of | RO |

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| | | | | |
|------|--------|---|-------|-----|
| | | PCI power management. 1: the ADM9511 provides the PCI management function 0: the ADM9511 doesn't provide New Capabilities. | CSR18 | |
| 19~9 | --- | Reserved | | |
| 8 | CSE | Command of System Error Response 1: enable system error response. ADM9511 will assert SERR# when it finds a parity error on the address phase. | 0 | R/W |
| 7 | --- | Reserved | | |
| 6 | CPE | Command of Parity Error Response 0: disable parity error response. ADM9511 will ignore any detected parity error and keep on its operating. Default value is 0. 1: enable parity error response. ADM9511 will assert system error (bit 13 of CSR5) when a parity error is detected. | 0 | R/W |
| 5~3 | --- | Reserved | | |
| 2 | CMO | Command of Master Operation Ability 0: disable the bus master ability. 1: enable the PCI bus master ability. Default value is 1 for normal operation. | 0 | R/W |
| 1 | CMSA | Command of Memory Space Access 0: disable the memory space access ability. 1: enable the memory space access ability. | 0 | R/W |
| 0 | CIOASA | Command of I/O Space Access 0: enable the I/O space access ability. 1: disable the I/O space access ability. | 0 | R/W |

R/W: Read and Write able. RO: Read able only.

MCR2 (offset = 108h), CC - Class Code and Revision Number

| Bit # | Name | Descriptions | Default Val | R/W Type |
|-------|------|---|-------------|----------|
| 31~24 | BCC | Base Class Code. It means the second function is a simple communication device. | 07h | RO |
| 23~16 | SC | Subclass Code. It means the second function is a modem device. | 00h | RO |
| 15~8 | --- | Reserved | | |
| 7 ~ 4 | RN | Revision Number, identifies the revision number of modem device | From EEPROM | RO |
| 3 ~ 0 | SN | Step Number, identifies the steps within the current revision. | From EEPROM | RO |

RO: Read Only.

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****MCR3 (offset = 10ch), LT - Latency Timer**

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~24 | ---- | reserved | | |
| 23~16 | HT | A value of 80h to indicate ADM9511 is a multiple function device for a combination of Ethernet and modem card. | 80h | RO |
| 15~ 8 | LT | Latency Timer. This value specifies the latency timer of the ADM9511 in units of PCI bus clock. Once the device asserts FRAME#, the latency timer starts to count. If the latency timer expires and the device still asserted FRAME#, then the device will terminate the data transaction as soon as its GNT# is removed. | 0 | R/W |
| 7 ~ 0 | CLS | Cache Line Size. This value specifies the system cache line size in units of 32-bit double words (DW). The ADM9511 supports 8, 16, and 32 DW of cache line size. This value is used by the ADM9511 driver to program the cache alignment bits(bit 14 and 15 of CSR0). The cache alignment bits are used for cache oriented PCI commands, say memory-read-line, memory-read-multiple, and memory-write-and-invalidate. | 0 | R/W |

MCR4 (offset = 110h), IOBA - I/O Base Address

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~ 8 | IOBA | I/O Base Address. This value indicate the base address of modem control and status registers | 0 | R/W |
| 7 ~ 1 | --- | Reserved | | |
| 0 | IOSI | I/O Space Indicator. 1: means that the configuration registers map into the I/O space. | 1 | RO |

MCR5 (offset = 14h), MBA - Memory Base Address

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|--|-------------|---------|
| 31~ 10 | MBA | Memory Base Address. This value indicate the base address of PCI control and status register | 0 | R/W |
| 9 ~ 1 | --- | Reserved | | |
| 0 | IOSI | Memory Space Indicator. | 0 | RO |

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| | | | | |
|--|--|--|--|--|
| | | 0: means that the configuration registers map into the memory space. | | |
|--|--|--|--|--|

MCR10 (offset = 28h), CIS - Card Information Structure

This register is used to point one of the possible address spaces where the CIS begins. This register is designed for PCI environment. It's data is auto-loaded from the serial EEPROM after power on or hardware reset.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~28 | RI | ROM Image. This ROM image value is applied when the CIS is stored in a boot ROM. This value is loaded from serial EEPROM. | From EEPROM | RO |
| 27~ 3 | ASO | Address Space Offset. This value indicates the offset within the address space. The address space is specified by address space indicator (bit 2~0 of MCR10). | From EEPROM | RO |
| 2 ~ 0 | ASI | Address Space Indicator. This value indicates the location where the CIS address space begins. 7: means that the CIS begins in the boot ROM space. Other than 7: makes all the bits of CIS reset to 0. | From EEPROM | RO |

MCR11 (offset = 12ch), SID - Subsystem ID.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | SID | Subsystem ID. This value is loaded from EEPROM after power on or hardware reset. | From EEPROM | RO |
| 15~ 0 | SVID | Subsystem Vendor ID. This value is loaded from EEPROM after power on or hardware reset. | From EEPROM | RO |

MCR12 (offset = 130h), BRBA - Boot ROM Base Address.

This register should be initialized before accessing the boot ROM space. (write 32'hffffff return 32'h fffe0001)

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|---|------------------------|---------|
| 31~17 | BRBA | Boot ROM Base Address. This value indicates the address mapping of boot ROM field. Besides, it also defines the boot ROM size. The value of bit 17~10 is set to 0 for ADM9511 supports up to 128kB of boot ROM. | X: b31~18 0: b17~10 | R/W |
| 16 ~ 1 | --- | Reserved | 0 | |

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| | | | | |
|---|-----|--|---|----|
| 0 | BRE | 0: disable Boot ROM. Modem device doesn't support Boot ROM. | 0 | RO |
|---|-----|--|---|----|

MCR13 (offset = 134h), CP - Capabilities Pointer.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|-----------------------|-------------|---------|
| 31~8 | --- | Reserved | | |
| 7~0 | CP | Capabilities Pointer. | C0h | RO |

MCR15 (offset = 13ch), CINT - Configuration Interrupt

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~24 | ML | Max_Lat register. This value indicates "how often" the ADM9511 needs to access to the PCI bus in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset. | From EEPROM | RO |
| 23~16 | MG | Min_Gnt register. This value indicates "how long" the ADM9511 needs to retain the PCI bus ownership whenever it initiates a transaction in the units of 250ns. This value is loaded from serial EEPROM after power on or hardware reset. | From EEPROM | RO |
| 15~ 8 | IP | Interrupt Pin. This value indicates which of the four interrupt request pins that ADM9511 is connected. Always 01h: means the ADM9511 connects to INTA# | 01h | RO |
| 7 ~ 0 | IL | Interrupt Line. This value indicates which of the system interrupt request lines the INTA# of ADM9511 is routed to. The BIOS will fill this field when it initializes and configures the system. The ADM9511 driver can use this value to determine priority and vector information. | X | R/W |

MCR16 (offset = 140h), DS - Driver Space for special purpose.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | --- | reserved | | |
| 15~8 | DS | Driver Space for special purpose. Since this area won't be cleared in the software reset. The ADM9511 driver can use this R/W area for special purpose. | X | R/W |
| 7 ~ 0 | --- | Reserved | | |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****MCR32 (offset = 180h), SIG - Signature of ADM9511**

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~16 | DID | Device ID, the device ID number of ADM9511. | 6985h | RO |
| 15~0 | VID | Vendor ID, the vendor ID number of ADM Technology Corp. | 1317h | RO |

MCR48 (offset = 1c0h), PMR0, Power Management Register0.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~27 | PMES | PME_Support. The ADM9511 will assert PME#/CSTSCHG signal while in the D0, D1, D2, D3hot power state. The ADM9511 supports Wake-up from the above four states. | 11111b | RO |
| 26 | D2S | D2_Support. The ADM9511 supports D2 Power Management State. | 1 | RO |
| 25 | D1S | D1_Support. The ADM9511 supports D1 Power Management State. | 1 | RO |
| 24~22 | AUXC | Aux. Current. These three bits report the maximum 3.3 Vaux current requirements for ADM9511. If bit 31 of PMR0 is '1', the default value is 0101b, means ADM9511 need 100 mA to support remote wake-up in D3cold power state. | 000b | RO |
| 21 | DSI | The Device Specific Initialization bit indicates whether special initialization of this function is required before the generic class device driver is able to use it. 0: indicates that the function does not require a device specific initialization sequence following transition to the D0 un-initialized state. | 0 | RO |
| 20 | --- | Reserved. | 0 | RO |
| 19 | PMEC | PME Clock. When "1" indicates that the ADM9511 relies on the presence of the PCI clock for PME#/CSTSCHG operation. While "0" indicates the no PCI clock is required for the ADM9511 to generate PME#/CSTSCHG. | 0 | RO |
| 18~16 | VER | Version. The value of 010b indicates that the ADM9511 complies with Revision 1.1 of the PCI Power Management Interface Specification. | 010b | RO |
| 15~8 | NIP | Next Item Pointer. This value is always 0h, indicates that there is no additional items in the Capabilities List. | 00h | RO |

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| | | | | |
|-----|-------|--|-----|----|
| 7~0 | CAPID | Capability Identifier. This value is always 01h, indicates the link list item as being PCI Power Management Registers. | 01h | RO |
|-----|-------|--|-----|----|

MCR49 (offset = 1c4h), PMR1, Power Management Register 1.

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|--------|---|-------------|---------|
| 31~24 | DR | Data register. This register is used to report the state dependent data requested by the data_select field. The value of this register is scaled by the value reported by the data_scale field | 0 | RO |
| 23~16 | ----- | Reserved | 8'b0 | RO |
| 15 | PMES | PME_Status, This bit is set when the ADM9511 would normally assert the PME#/CSTSCHG signal for wake-up event, this bit is independent of the state of the PME-En bit. Writing a "1" to this bit will clear it and cause the ADM9511 to stop asserting a PME#/CSTSCHG (if enabled). Writing a "0" has no effect. | 0 | R/W* |
| 14,13 | DSCAL | Data_Scale, indicates the scaling factor to be used when interpreting the value of the Data register. | 0 | RO |
| 12~9 | DSEL | Data_Select, This four bit field is used to select which data is to be reported through the Data register and Data_Scale field. | 0 | R/W |
| 8 | PME_En | PME_En, "1" enables the ADM9511 to assert PME#/CSTSCHG. When "0" disables the PME#/CSTSCHG assertion. | 0 | R/W |
| 7~2 | --- | reserved | 6'b000000 | RO |
| 1,0 | PWRS | Power State. This two-bit field is used both to determine the current power state of the ADM9511 and to set the ADM9511 into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 11b - D3hot This field is auto cleared to D0 when power resumed . | 00b | R/W |

R/W*: Read and Write clear

Modem data register :

| Data select | Data scale | Value | Data reported |
|-------------|------------|-------|----------------------|
| 0 | 2 | TBD | D0 power consumption |
| 1 | 2 | TBD | D1 power consumption |
| 2 | 2 | TBD | D2 power consumption |
| 3 | 2 | TBD | D3 power consumption |
| 4 | 2 | TBD | D0 power dissipated |

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| | | | |
|------|---|-----|----------------------------------|
| 5 | 2 | TBD | D1 power dissipated |
| 6 | 2 | TBD | D2 power dissipated |
| 7 | 2 | TBD | D3 power dissipated |
| 8 | 2 | TBD | Common function power dissipated |
| 9-15 | 2 | TBD | Reserved |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****8.2.Control/Status Registers****8.2.1. Ethernet Control/Status registers**

The base address of Ethernet Control/Status registers (CSRs) is specified in Function 0 PCI configuration registers.

8.2.1.1. Ethernet Control/Status registers list

| offset from base address of CSR | Index | Name | Descriptions |
|---------------------------------|--------|--------|--|
| 00h | CSR0 | PAR | PCI access register |
| 08h | CSR1 | TDR | Transmit demand register |
| 10h | CSR2 | RDR | Receive demand register |
| 18h | CSR3 | RDB | Receive descriptor base address |
| 20h | CSR4 | TDB | Transmit descriptor base address |
| 28h | CSR5 | SR | Status register |
| 30h | CSR6 | NAR | Network access register |
| 38h | CSR7 | IER | Interrupt enable register |
| 40h | CSR8 | LPC | Lost packet counter |
| 48h | CSR9 | SPR | Serial port register |
| 50h | CSR10 | --- | Reserved |
| 58h | CSR11 | TMR | General purpose timer |
| 60h | CSR12 | --- | Reserved |
| 68h | CSR13 | WCSR | Wake-up control/status register |
| 70h | CSR14 | WPDR | Wake-up pattern data register |
| 78h | CSR15 | WTMR | Watchdog timer |
| 7ch | CSR15a | CISCNT | CIS word count register |
| 80h | CSR16 | ACSR5 | Assistant CSR5 (Status register 2) |
| 84h | CSR17 | ACSR7 | Assistant CSR7 (Interrupt enable register 2) |
| 88h | CSR18 | CR | Command register |
| 8ch | CSR19 | PCIC | PCI bus performance counter |
| 90h | CSR20 | PMCSR | Power management command and status |
| 94h | CSR21 | WTDP | Current transmit descriptor point |
| 98h | CSR22 | WRDP | Current receive descriptor point |
| 9ch | CSR23 | TXBR | Transmit burst counter/time-out register |
| a0h | CSR24 | FROM | Flash(boot) ROM port |
| a4h | CSR25 | PAR0 | Physical address register 0 |
| a8h | CSR26 | PAR1 | Physical address register 1 |
| ach | CSR27 | MAR0 | Multicast address hash table register 0 |

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| | | | |
|-----------|-------|--------|---|
| b0h | CSR28 | MAR1 | Multicast address hash table register 1 |
| b4h | CSR29 | MDMCTL | Modem control register |
| fch | CSR30 | MCMR | Misc controller mode register |
| 100h | CSR31 | FER | Function event register |
| 104h | CSR32 | FEMR | Function event mask register |
| 108h | CSR33 | FPSR | Function present state register |
| 10ch | CSR34 | FFER | Function force event register |
| 200h~2FFh | | | Ethernet CIS area (load from EEPROM) |

8.2.1.2. Ethernet Control/Status registers description**CSR0 (offset = 00h), PAR - PCI Access Register**

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|---|-------------|---------|
| 31~25 | --- | Reserved | | |
| 24 | MWIE | Memory Write and Invalidate Enable. 1: Enable ADM9511 to generate memory write invalidate command. ADM9511 will generate this command while writing full cache lines. 0: Disable ADM9511 to generate memory write invalidate command and use memory write commands instead. | 0 | R/W* |
| 23 | MRLE | Memory Read Line Enable. 1: Enable ADM9511 to generate memory read line command, while read access instruction reach the cache line boundary. If the read access instruction doesn't reach the cache line boundary then ADM9511 uses the memory read command instead. | 0 | R/W* |
| 22 | --- | Reserved | | |
| 21 | MRME | Memory Read Multiple Enable. 1: Enable ADM9511 to generate memory read multiple command while reading full cache line. If the memory is not cache aligned, the ADM9511 uses memory read command instead. | 0 | R/W* |
| 20~19 | --- | Reserved | | |
| 18,17 | TAP | Transmit auto-polling in transmit suspended state, 00: disable auto-polling (default) 01: polling own-bit every 200 us 10: polling own-bit every 800 us 11: polling own-bit every 1600 us | 00 | R/W* |
| 16 | --- | Reserved | | |
| 15, 14 | CAL | Cache alignment, address boundary for data burst, set after reset 00: = PBL on bits 13~8 of CSR0 | 00 | R/W* |

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| | | | | |
|--------|-----|--|--------|------|
| | | 01: the minimum value of (8 DW , PBL) 10: the minimum value of (16 DW, PBL) 11: the minimum value of (32 DW , PBL) | | |
| 13 ~ 8 | PBL | Programmable Burst Length. This value defines the maximum number of DW to be transferred in one DMA transaction. value: 0 (unlimited), 1, 2, 4, 8, 16(default), 32 DW | 010000 | R/W* |
| 7 | BLE | Big or Little endian selection. 0: little endian (e.g. INTEL) 1: big endian (only for data buffer) | 0 | R/W* |
| 6 ~ 2 | DSL | Descriptor Skip Length. Defines the gap between two descriptions in the units of DW. | 0 | R/W* |
| 1 | BAR | Bus arbitration 0: receive higher priority 1: transmit higher priority | 0 | R/W* |
| 0 | SWR | Software reset 1: reset all internal hardware, except configuration registers. This signal will be cleared by ADM9511 itself after it completed the reset process. | 0 | R/W* |

R/W* = Before writing the register, the transmit and receive operations should be stopped.

CSR1 (offset = 08h), TDR - Transmit demand register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~0 | TPDM | Transmit poll demand When written any value in suspended state, trigger read-tx-descriptor process and check the own-bit, if own-bit = 1, then start transmit process | fffffffh | R/W* |

R/W* = Before writing the register, the transmit process should be in the suspended state.

CSR2 (offset = 10h), RDR - Receive demand register

| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|------|--|-------------|---------|
| 31 ~ 0 | RPDM | Receive poll demand When written any value in suspended state, trigger the read-rx-descriptor process and check own-bit, if own-bit = 1, then start move data to buffer from FIFO | fffffffh | R/W* |

R/W* = Before writing the register, the receive process should be in the suspended state.

CSR3 (offset = 18h), RDB - Receive descriptor base address

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--------------|-------------|---------|
|-------|------|--------------|-------------|---------|

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| | | | | |
|------|------|-------------------------------------|---------|------|
| 31~2 | SAR | Start address of receive descriptor | xxxxxxx | R/W* |
| 1, 0 | RBND | must be 00, DW boundary | 00 | RO |

R/W* = Before writing the register, the receive process should be stopped.

CSR4 (offset = 20h), TDB - Transmit descriptor base address

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--------------------------------------|-------------|---------|
| 31~2 | SAT | Start address of transmit descriptor | xxxxxxx | R/W* |
| 1, 0 | TBND | must be 00, DW boundary | 00 | RO |

R/W* = Before writing the register, the transmit process should be stopped.

CSR5 (offset = 28h), SR - Status register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~26 | ---- | reserved | | |
| 25~23 | BET | Bus Error Type. This field is valid only when bit 13 of CSR5 (fatal bus error) is set. There is no interrupt generated by this field. 000: parity error, 001: master abort, 010: target abort others: reserved | 000 | RO |
| 22~20 | TS | Transmit State. Report the current transmission state only, no interrupt will be generated. 000: stop 001: read descriptor 010: transmitting 011: FIFO fill, read the data from memory and put into FIFO 100: reserved 101: reserved 110: suspended, unavailable transmit descriptor or FIFO overflow 111: write descriptor | 000 | RO |
| 19~17 | RS | Receive State. Report current receive state only, no interrupt will be generated. 000: stop 001: read descriptor 010: check this packet and pre-fetch next descriptor 011: wait for receiving data 100: suspended 101: write descriptor 110: flush the current FIFO 111: FIFO drain, move data from receiving FIFO into memory | 000 | RO |
| 16 | NISS | Normal Interrupt Status Summary. It's set if any of below | 0 | RO/LH* |

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| | | | | |
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| | | bits of CSR5 asserted.(combines with bit 16 of ACSR5) bit0, transmit completed interrupt bit2, transmit descriptor unavailable bit6, receive descriptor interrupt | | |
| 15 | AISS | Abnormal Interrupt Status Summary. It's set if any of below bits of CSR5 asserted.(combines with bit 15 of ACSR5) bit1, transmit process stopped bit3, transmit jabber timer time-out bit5, transmit under-flow bit7, receive descriptor unavailable bit8, receive processor stopped bit9, receive watchdog time-out bit11, general purpose timer time-out bit13, fatal bus error | 0 | RO/LH* |
| 14 | ---- | reserved | | |
| 13 | FBE | Fatal Bus Error. 1: while any of parity error, master abort, or target abort is occurred (see bits 25~23 of CSR5). ADM9511 will disable all bus access. The way to recover parity error is by setting an software reset. | 0 | RO/LH* |
| 12 | --- | Reserved | | |
| 11 | GPTT | General Purpose Timer Time-out, base on CSR11 timer register | 0 | RO/LH* |
| 10 | --- | Reserved | | |
| 9 | RWT | Receive Watchdog Time-out, based on CSR15 watchdog timer register | 0 | RO/LH* |
| 8 | RPS | Receive Process Stopped, receive state = stop | 0 | RO/LH* |
| 7 | RDU | Receive Descriptor Unavailable 1: while the next receive descriptor can't be applied by ADM9511, the receive process is suspended in this situation. To restart the receive process, the ownership bit of next receive descriptor should be set to ADM9511 and a receive poll demand command should be issued(or a new recognized frame is received, if the receive poll demand is not issued). | 0 | RO/LH* |
| 6 | RCI | Receive Completed Interrupt 1: while a frame reception is completed. | 0 | RO/LH* |
| 5 | TUF | Transmit Under-Flow 1: while the transmit FIFO had an under-flow condition happened during transmitting, the transmit process will enter the suspended state and report the under-flow error on bit 1 of TDES0. | 0 | RO/LH* |
| 4 | --- | Reserved | | |
| 3 | TJT | Transmit Jabber Time-out | 0 | RO/LH* |

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| | | 1: while the transmit jabber timer expired, the transmit processor will enter the stop state and the transmit jabber time-out flag of bit 14 of TDES0 will be asserted. | | |
| 2 | TDU | Transmit Descriptor Unavailable 1: while the next transmit descriptor can't be applied by ADM9511. The transmission process is suspended in this situation. To restart the transmission process, the ownership bit of next transmit descriptor should be set to ADM9511 and if the transmit automatic polling is not enabled then a transmit poll demand command should be issued. | 0 | RO/LH* |
| 1 | TPS | Transmit Process Stopped. 1: while transmit state = stop | 0 | RO/LH* |
| 0 | TCI | Transmit Completed Interrupt. 1: means a frame transmission is completed while bit 31 of TDES1 is asserted in the first transmit descriptor of the frame. | 0 | RO/LH* |

LH = High Latching and cleared by writing 1.

CSR6 (offset = 30h), NAR - Network access register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~22 | --- | Reserved | | |
| 21 | SF | Store and forward for transmit 0: disable 1: enable, ignore the transmit threshold setting | 0 | R/W* |
| 20 | --- | Reserved | | |
| 19 | SQE | SQE Disable 0: enable SQE function for 10BASE-T operation. The ADM9511 provides SQE test function for 10BASE-T half duplex operation. 1: disable SQE function. | 1 | R/W* |
| 18~16 | ---- | Reserved | | |
| 15~14 | TR | transmit threshold control 00: 128-byte (100Mbps), 72-byte (10Mbps) 01: 256-byte (100Mbps), 96-byte (10Mbps) 10: 512-byte (100Mbps), 128-byte (10Mbps) 00: 1024-byte (100Mbps), 160-byte (10Mbps) | 00 | R/W* |
| 13 | ST | Stop transmit 0: stop (default) 1: start | 0 | R/W |
| 12 | FC | Force collision mode 0: disable 1: generate collision when transmit (for test in loop-back) | 0 | R/W** |

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| | | mode) | | |
| 11, 10 | OM | Operating Mode 00: normal 01: MAC loop-back 10,11: reserved | 00 | R/W** |
| 9, 8 | --- | Reserved | | |
| 7 | MM | Multicast Mode 1: receive all multicast packets | 0 | R/W*** |
| 6 | PR | Promiscuous Mode 1: receive any good packet. 0: receive only the right destination address packets | 1 | R/W*** |
| 5 | SBC | Stop Back-off Counter 1: back-off counter stop when carrier is active, and resume when carrier drop. 0: back-off counter is not effected by carrier | 0 | R/W** |
| 4 | — | Reserved | | |
| 3 | PB | Pass Bad packet 1: receives any packets, if pass address filter, including runt packets, CRC error, truncated packets... For receiving all bad packets, the bit 6 of CSR6 should be set to 1. 0: filters all bad packets | 0 | R/W*** |
| 2 | — | Reserved | | |
| 1 | SR | Start/Stop Receive 0: receive processor will enter stop state after the current reception frame completed. This value is effective only when the receive processor is in the running or suspending state. Notice: In “Stop Receive” state, the PAUSE packet and Remote Wake Up packet won't be effected and can be received if the corresponding function is enabled. 1: receive processor will enter running state. | 0 | R/W |
| 0 | --- | Reserved | | |

W* = only write when the transmit processor stopped.

W = only write when the transmit and receive processor both stopped.**

W* = only write when the receive processor stopped.**

CSR7 (offset = 38h), IER - Interrupt Enable Register

| Bit # | Name | Descriptions (Refer to CSR5) | Default Val | RW Type |
|-------|-------|--|-------------|---------|
| 31~17 | --- | Reserved | | |
| 16 | NIE | Normal Interrupt Enable 1: enable all the normal interrupt bits(see bit16 of CSR5) | 0 | R/W |
| 15 | AIE | Abnormal Interrupt Enable 1: enable all the abnormal interrupt bits(see bit 15 of CSR5) | 0 | R/W |
| 14 | --- | Reserved | | |
| 13 | FBEIE | Fatal Bus Error Interrupt Enable | 0 | R/W |

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| | | | | |
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| | | 1: combine this bit and bit 15 of CSR7 to enable fatal bus error interrupt | | |
| 12 | | | | |
| 11 | GPTIE | General Purpose Timer Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable the general purpose timer expired interrupt. | 0 | R/W |
| 10 | --- | Reserved | | |
| 9 | RWTIE | Receive Watchdog Time-out Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive watchdog time-out interrupt. | 0 | R/W |
| 8 | RSIE | Receive Stopped Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive stopped interrupt. | 0 | R/W |
| 7 | RUIE | Receive Descriptor Unavailable Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable receive descriptor unavailable interrupt. | 0 | R/W |
| 6 | RCIE | Receive Completed Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable receive completed interrupt. | 0 | R/W |
| 5 | TUIE | Transmit Under-flow Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit under-flow interrupt. | 0 | R/W |
| 4 | --- | Reserved | | |
| 3 | TJTIE | Transmit Jabber Timer Time-out Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit jabber timer time-out interrupt. | 0 | R/W |
| 2 | TDUIE | Transmit Descriptor Unavailable Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable transmit descriptor unavailable interrupt. | 0 | R/W |
| 1 | TPSIE | Transmit Processor Stopped Interrupt Enable 1: combine this bit and bit 15 of CSR7 to enable transmit processor stopped interrupt. | 0 | R/W |
| 0 | TCIE | Transmit Completed Interrupt Enable 1: combine this bit and bit 16 of CSR7 to enable transmit completed interrupt. | 0 | R/W |

CSR8 (offset = 40h), LPC - Lost packet counter

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~17 | --- | Reserved | | |
| 16 | LPCO | Lost Packet Counter Overflow 1: while lost packet counter overflowed. It will be cleared after read | 0 | RO/LH |

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|------|-----|--|---|-------|
| 15~0 | LPC | Lost Packet Counter InMCRent the counter while a packet discarded due to there was no host receive descriptors available. It will be cleared after read | 0 | RO/LH |
|------|-----|--|---|-------|

CSR9(offset = 48h), SPR - Serial port register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~20 | --- | Reserved | | |
| 19 | MDI | MII Management Data Input Specified read data from the external PHY | 0 | R/W |
| 18 | MMC | MII Management Control 0: Write operation to the external PHY 1: Read operation from the external PHY | 1 | R/W |
| 17 | MDO | MII Management Data Output Specified Write Data to the external PHY | 0 | R/W |
| 16 | MDC | MII Management Clock 1: MII Management Clock is a output reference clock to the external PHY | 0 | R/W |
| 15 | --- | Reserved | | |
| 14 | SRC | Serial EEPROM Read Control Set together with bit 11 of CSR9 to enable read operation from EEPROM | 0 | R/W |
| 13 | SWC | Serial EEPROM Write Control Set together with bit 11 of CSR9 to enable write operation to EEPROM | 0 | R/W |
| 12 | --- | Reserved | | |
| 11 | SRS | Serial EEPROM Select Set together with bit 14 or 13 of CSR9 to enable EEPROM access | 0 | R/W |
| 10~4 | --- | Reserved | | |
| 3 | SDO | Serial EEPROM data out This bit serially shifts data from the EEPROM to the ADM9511 | 1 | RO |
| 2 | SDI | Serial EEPROM data in This bit serially shifts data from the ADM9511 to the EEPROM. | 1 | R/W |
| 1 | SCLK | Serial EEPROM clock High/Low this bit to provide the clock signal for EEPROM. | 1 | R/W |
| 0 | SCS | Serial EEPROM chip select 1: selects the serial EEPROM chip. | 0 | R/W |

CSR11 (offset = 58h), TMR -General-purpose Timer**ADMtek Inc.**

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| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~17 | --- | Reserved | | |
| 16 | COM | Continuous Operation Mode 1: sets the general-purpose timer in continuous operating mode. | 0 | R/W |
| 15~0 | GTV | General-purpose Timer Value Sets the counter value. This is a count-down counter with the cycle time of 204us. | 0 | R/W |

CSR13 (offset = 68h), WCSR –Wake-up Control/Status Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------|--|-------------|---------|
| 31 | --- | Reserved | | |
| 30 | CRCT | CRC-16 Type 0: Initial contents = 0000h 1: Initial contents = FFFFh | 0 | R/W |
| 29 | WP1E | Wake-up Pattern One Matched Enable. | 0 | R/W |
| 28 | WP2E | Wake-up Pattern Two Matched Enable. | 0 | R/W |
| 27 | WP3E | Wake-up Pattern Three Matched Enable. | 0 | R/W |
| 26 | WP4E | Wake-up Pattern Four Matched Enable. | 0 | R/W |
| 25 | WP5E | Wake-up Pattern Five Matched Enable. | 0 | R/W |
| 24-18 | --- | Reserved | | |
| 17 | LinkOFF | Link Off Detect Enable. The ADM9511 will set the LSC bit of CSR13 after it has detected that link status is from ON to OFF. | 0 | R/W |
| 16 | LinkON | Link On Detect Enable. The ADM9511 will set the LSC bit of CSR13 after it has detected that link status is from OFF to ON. | 0 | R/W |
| 15-11 | --- | Reserved | 00001 | |
| 10 | WFRE | Wake-up Frame Received Enable. The ADM9511 will include the “Wake-up Frame Received” event into wake-up events. If this bit is set, ADM9511 will assert PMES bit of PMR1 after ADM9511 has received a matched wake-up frame. | 0 | R/W |
| 9 | MPRE | Magic Packet Received Enable. The ADM9511 will include the “Magic Packet Received” event into wake-up events. If this bit is set, ADM9511 will assert PMES bit of PMR1 after ADM9511 has received a Magic packet. | 0 | R/W |
| 8 | LSCE | Link Status Changed Enable. The ADM9511 will include the “Link Status Changed” event into wake-up events. If this bit is set, ADM9511 will assert PMES bit of PMR1 after ADM9511 has detected a link status changed event. | 0 | R/W |
| 7-3 | --- | Reserved | | |

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| | | | | |
|---|-----|--|---|--------|
| 2 | WFR | Wake-up Frame Received, 1: Indicates ADM9511 has received a wake-up frame. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset. | X | R/W1C* |
| 1 | MPR | Magic Packet Received, 1: Indicates ADM9511 has received a magic packet. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset. | X | R/W1C* |
| 0 | LSC | Link Status Changed, 1: Indicates ADM9511 has detected a link status change event. It is cleared by write 1 or upon power-up reset. It is not affected by a hardware or software reset. | X | R/W1C* |

R/W1C*, Read Only and Write one to clear.

CSR14 (offset = 70h), WPDR –Wake-up Pattern Data Register

All six wake-up patterns filtering information are programmed through WPDR register. The filtering information is as follows

| | | | |
|-------|------------------------------------|----------|--------------------------|
| 0000h | Wake-up pattern 1 mask bits 31:0 | | |
| 0004h | Wake-up pattern 1 mask bits 63:32 | | |
| 0008h | Wake-up pattern 1 mask bits 95:64 | | |
| 000ch | Wake-up pattern 1 mask bits 127:96 | | |
| 0010h | CRC16 of pattern 1 | Reserved | Wake-up pattern 1 offset |
| 0014h | Wake-up pattern 2 mask bits 31:0 | | |
| 0018h | Wake-up pattern 2 mask bits 63:32 | | |
| 001ch | Wake-up pattern 2 mask bits 95:64 | | |
| 0020h | Wake-up pattern 2 mask bits 127:96 | | |
| 0024h | CRC16 of pattern 2 | Reserved | Wake-up pattern 2 offset |
| 0028h | Wake-up pattern 3 mask bits 31:0 | | |
| 002ch | Wake-up pattern 3 mask bits 63:32 | | |
| 0030h | Wake-up pattern 3 mask bits 95:64 | | |
| 0034h | Wake-up pattern 3 mask bits 127:96 | | |
| 0038h | CRC16 of pattern 3 | Reserved | Wake-up pattern 3 offset |
| 003ch | Wake-up pattern 4 mask bits 31:0 | | |
| 0040h | Wake-up pattern 4 mask bits 63:32 | | |
| 0044h | Wake-up pattern 4 mask bits 95:64 | | |
| 0048h | Wake-up pattern 4 mask bits 127:96 | | |
| 004ch | CRC16 of pattern 4 | Reserved | Wake-up pattern 4 offset |
| 0050h | Wake-up pattern 5 mask bits 31:0 | | |
| 0054h | Wake-up pattern 5 mask bits 63:32 | | |
| 0058h | Wake-up pattern 5 mask bits 95:64 | | |
| 005ch | Wake-up pattern 5 mask bits 127:96 | | |
| 0060h | CRC16 of pattern 5 | Reserved | Wake-up pattern 5 offset |

1. Offset value is from 0-255 (8-bit width).

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2. To load the whole wake-up frame filtering information, consecutive 25 long words write operation to CSR14 should be done.

CSR15 (offset = 78h), WTMR - Watchdog timer

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~6 | --- | Reserved | | |
| 5 | RWR | Receive Watchdog Release, the time of release watchdog timer from last carrier deserted. 0: 24 bit-time 1: 48 bit-time | 0 | R/W |
| 4 | RWD | Receive Watchdog Disable 0: If the receiving packet's length is longer than 2560 bytes, the watchdog timer will be expired. 1: disable the receive watchdog. | 0 | R/W |
| 3 | --- | Reserved | | |
| 2 | JCLK | Jabber clock 0: cut off transmission after 2.6 ms (100Mbps) or 26 ms (10Mbps). 1: cut off transmission after 2560 byte-time. | 0 | R/W |
| 1 | NJ | Non-Jabber 0: if jabber expired, re-enable transmit function after 42 ms (100Mbps) or 420ms (10Mbps) 1: immediately re-enable the transmit function after jabber expired | 0 | R/W |
| 0 | JBD | Jabber disable 1: disable transmit jabber function | 0 | R/W |

CSR15a (offset = 7ch), CISCNT – CIS word count register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------|---------------------|-------------|---------|
| 31-16 | --- | Reserved | | |
| 15-8 | MCIScnt | MODEM CIS length | From EEPROM | RO |
| 7-0 | CIScnt | Ethernet CIS length | From EEPROM | RO |

CSR16 (offset = 80h), ACSR5 - Assistant CSR5 (Status register 2)

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31 | TEIS | Transmit Early Interrupt status Transmit early interrupt status is set to 1 when Transmit early interrupt function is enabled (set bit 31 of CSR17 = 1) and the transmitted packet is moved completed from descriptors to | 0 | RO/LH* |

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| | | TX-FIFO buffer. This bit is cleared by written with 1. | | |
| 30 | REIS | Receive Early Interrupt Status. Receive early interrupt status is set to 1 when Receive early interrupt function is enabled (set bit 30 of CSR17 = 1) and the received packet is fill up its first receive descriptor. This bit is cleared by written with 1. | 0 | RO/LH* |
| 29 | LCS | Status of link status change | 0 | RO/LH* |
| 28 | TDIS | Transmit Deferred Interrupt Status. | 0 | RO/LH* |
| 27 | --- | Reserved | | |
| 26 | PFR | PAUSE Frame Received Interrupt Status 1: indicates a PAUSE frame received when the PAUSE function is enabled. | 0 | RO/LH* |
| 25~17 | --- | Reserved | | |
| 16 | ANISS | Added normal interrupt status summary. 1: any of the added normal interrupt happened. | 0 | RO/LH* |
| 15 | AAISS | Added Abnormal Interrupt Status Summary. 1: any of added abnormal interrupt happened. | 0 | RO/LH* |
| 14~0 | | These bits are the same as the status register of CSR5. You can access those status bits through either CSR5 or CSR15a. | | RO/LH* |

LH* = High Latching and cleared by writing 1.

CSR17 (offset = 84h), ACSR7- Assistant CSR7(Interrupt enable register 2)

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------|---|-------------|---------|
| 31 | TEIE | Transmit Early Interrupt Enable | 0 | R/W |
| 30 | REIE | Receive Early Interrupt Enable | 0 | R/W |
| 29 | LCIE | Link Change Interrupt enable | 0 | R/W |
| 28 | TDIE | Transmit Deferred Interrupt Enable | 0 | R/W |
| 27 | --- | Reserved | | |
| 26 | PFRIE | PAUSE Frame Received Interrupt Enable | 0 | R/W |
| 25~17 | --- | Reserved | | |
| 16 | ANISE | Added Normal Interrupt Summary Enable. 1: adds the interrupts of bit 30 and 31 of ACSR7 to the normal interrupt summary (bit 16 of CSR5). | 0 | R/W |
| 15 | AAIE | Added Abnormal Interrupt Summary Enable. 1: adds the interrupt of bit 26, 28 and 29 of ACSR7 to the abnormal interrupt summary (bit 15 of CSR5). | 0 | R/W |
| 14~0 | | These bits are the same as the interrupt enable register of CSR7. You can access those interrupt enable bits through either CSR7 or CSR17. | | R/W |

CSR18 (offset = 88h), CR - Command Register, bit31 to bit16 automatically recall from EEPROM

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| Bit # | Name | Descriptions | Default Val | RW Type |
|--------|-------------|--|------------------------|---------|
| 31 | D3CS | D3cold support , mapped to CR48<31> | 1 from EEPROM | R/W |
| 30-28 | AUXCL | Aux Current. These three bits report the maximum 3.3 Vaux current requirements for ADM9511. If bit 31 of PMR0 is '1', the default value is 0101b, means ADM9511 need 100 mA to support remote wake-up in D3cold power state | 000b from EEPROM | R/W |
| 27 | pmepsel | This bit control the polarity of PMEP pin 1 : PMEP output a negtive pulse; 0 : PMEP output a positive pulse | 0 from EEPROM | R/W |
| 26 | -- | Reserved | | |
| 25 | Pci_pad | This bit is only effective in Cardbus mode, it is no effect in PCI mode 1 : Output PCI pad to the Cardbus interface 0 : Output Cardbus pad to the CardBus interface | 0 from eeprom | R/W |
| 24 | Pmes_sticky | 1 : pmez sticky: While pmez signal is asserted by wake up event, it can not be auto de-asserted. The software should clear CR49<15> PMES bit to de-assert the pmez signal. 0 : pmez auto de-asserted. While pmez signal is asserted by wake up event, it will be de-asserted by power up automatically. | 0 from eeprom | R/W |
| 23 | 4_3LED | If this bit is reset, 3 LED mode is selected, the LEDs definition is: ● 100/10 speed ● Link/Activity ● Full Duplex/Collision If this bit is set, 4 LED mode is selected, the LEDs definition is: ● 100 Link ● 10 Link ● Activity ● Full Duplex/Collision | 0 from EEPROM | R/W |
| 22, 21 | RFS | Receive FIFO size control 11: 1K 10: 2K 01,00: reserved | 10 from EEPROM | R/W |
| 20 | CRD | Clock Run (clk-run pin) disable 1: disables the function of clock run supports to PCI. | 0 from EEPROM | R/W |
| 19 | PM | Power Management, enables the ADM9511 whether to activate the Power Management abilities. When this bit is set into "0" the ADM9511 will set the Cap_Ptr register to zero, indicating no PCI compliant power management capabilities. | 1 from EEPROM | RO |

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| | | | | |
|------|-----------|--|---------------------|-----|
| | | The value of this bit will be mapped to NC-bit 20 of CR1. In PCI Power Management mode, the Wake-up events include “Wake-up Frame Received”, “Magic Packet Received” and “Link Status Changed” depends on the CSR13 settings | | |
| 18 | APM | APM mode , this bit is effective when CSR18[19] PM bit is set. 1: Magic packet wake-up event default enable 0: Magic packet wake-up event default disable | 1 from EEPROM | R/W |
| 17 | LWS | Should be 0 | 0 from EEPROM | R/W |
| 16~9 | ---- | Reserved | | |
| 8 | Pmepshort | PMEP pulse length 0: The pulse width of PMEP is 50ms 1: The pulse width of PMEP is set to short pulse 100us for test purpose | 0 | R/W |
| 7 | D3_APM | This bit is used to force generating pmez signal. It doesn't care the PME_EN status, the pmez signal can be asserted by programming this bit 1: Assert pmez signal 0: De-assert pmez signal | 0 | R/W |
| 6 | RWP | Reset Wake-up Pattern Data Register Pointer 0: Normal 1: Reset | 0 | R/W |
| 5 | PAUSE | PAUSE function control to disable or enable the PAUSE function for flow control. The default value of PAUSE is decided by the result of Auto-Negotiation. Driver can force to enable or disable it after the Auto-Negotiation completed. 0: PAUSE function is disabled. 1: PAUSE function is enabled | 0 | R/W |
| 4 | RTE | Receive Threshold Enable. 1: the receive FIFO threshold is enabled. 0: disable the receive FIFO threshold selection in bit 3~2 of this register, the receive threshold is set to 64-byte. | 0 | R/W |
| 3~2 | DRT | Drain Receive Threshold 00: 32 bytes (8 DW) 01: 64 bytes (16 DW) 10: store-and-forward 11: reserved | 01 | R/W |
| 1 | SINT | Software interrupt | 0 | R/W |
| 0 | ATUR | 1: enable automatically transmit-underrun recovery. | 0 | R/W |

CSR19(offset = 8ch) - PCIC, PCI bus performance counter**ADMtek Inc.**

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| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|--------|--|-------------|---------|
| 31~16 | CLKCNT | The number of PCI clock from read request asserted to access completed. This PCI clock number is accumulated all the read command cycles from last CSR19 read to current CSR19 read. | 0 | RO* |
| 15~8 | --- | reserved | | |
| 7~0 | DWCNT | The number of double word accessed by the last bus master. This double word number is accumulated all the bus master data transactions from last CSR19 read to current CSR19 read. | 0 | RO* |

RO* = Read only and cleared by reading.

CSR20 (offset = 90h) - PMCSR, Power Management Command and Status.(The same register value mapping to CR49-PMR1.)

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|--------|--|-------------|---------|
| 31~16 | --- | reserved | | |
| 15 | PMES | PME_Status, This bit is set when the ADM9511 would normally assert the PME# signal for wakeup event, this bit is independent of the state of the PME_En bit. Writing a "1" to this bit will clear it and cause the ADM9511 to stop asserting a PME#(if enabled). Writing a "0" has no effect. | 0 | R/W |
| 14,13 | DSCAL | Data_Scale, indicates the scaling factor to be used when interpreting the value of the Data register. | 00b | RO |
| 12~9 | DSEL | Data_Select, This four-bit field is used to select which data is to be reported through the Data register and Data_Scale field. | 0000b | R/W |
| 8 | PME_En | PME_En, "1" enables the ADM9511 to assert PME#/CSTSCHG. When "0" disables the PME#/CSTSCHG assertion. Magic packet default enable: When CSR18<18> and CSR18<19> are set to 1, then the magic packet wake up event will be default enabled (CSR13<9> be set), it doesn't matter the PME_En is set or not. | 0 | RO |
| 7~2 | --- | reserved | 000000b | RO |
| 1,0 | PWRS | Power State. This two-bit field is used both to determine the current power state of the ADM9511 and to set the ADM9511 into a new power state. The definition of this field is given below. 00b - D0 01b - D1 10b - D2 | 00b | RO |

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| | | | | |
|--|--|--|--|--|
| | | 11b - D3hot This field is auto cleared to D0 when power resumed . | | |
|--|--|--|--|--|

CSR21 (offset = 94h) - WTDP, The current working transmit descriptor pointer

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~0 | WTDP | The current working transmit descriptor pointer for driver's double check or other special purpose. | XXXX | RO |

CSR22 (offset = 98h) - WRDP, The current working receive descriptor pointer

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--|-------------|---------|
| 31~0 | WRDP | The current working receive descriptor pointer for driver's double check or other special purpose. | XXXX | RO |

CSR23 (offset = 9ch) - TXBR, transmit burst counter / time-out

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------|--|-------------|---------|
| 31~21 | --- | Reserved | | |
| 20~16 | TBCNT | Transmit Burst Count After this number of consecutive successful transmit, transmit completed interrupt will be generated. Continuously do this function if no reset. | 0 | R/W |
| 11~0 | TTO | Transmit Time-Out = (deferred time + back-off time). When the TDIE(bit28 of ACSR7) is set, the timer is decreased in unit of 2.56us(100M) or 25.6us(10M). If the timer expires before another packet transmit begin, then the TDIE interrupt will be generated. | 0 | R/W |

CSR24 (offset = a0h) - FROM, Flash ROM(also the boot ROM) port

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|----------|---|-------------|---------|
| 31 | Bra16_on | This bit is only effective when 4 LED mode selected (bit 23 of CSR18 is set). When 4 LED mode selected, and this bit is set, then pin G14, BrA16/LED-4 is defined as BrA16, otherwise, it is defined as LED pin – FD/COL | 1 | R/W |
| 30~28 | --- | Reserved | | |
| 27 | REN | read enable, clear if read data is ready in DATA, bit7-0 of FROM. | 0 | R/W |
| 26 | WEN | Write enable, cleared if write completed | 0 | R/W |
| 25~8 | ADDR | Flash ROM address | 0 | R/W |

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| | | | | |
|-----|------|------------------------------|---|-----|
| 7~0 | DATA | Read/Write data of flash ROM | 0 | R/W |
|-----|------|------------------------------|---|-----|

CSR25 (offset = a4h) - PAR0, physical address register 0, automatically recall from EEPROM

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|-------------------------|-------------|---------|
| 31~24 | PAB3 | physical address byte 3 | From EEPROM | R/W |
| 23~16 | PAB2 | physical address byte 2 | From EEPROM | R/W |
| 15~8 | PAB1 | physical address byte 1 | From EEPROM | R/W |
| 7~0 | PAB0 | physical address byte 0 | From EEPROM | R/W |

CSR26 (offset = a8h) - PAR1, physical address register 1, automatically recall from EEPROM

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|-------------------------|-------------|---------|
| 31~24 | --- | Reserved | | |
| 23~16 | --- | Reserved | | |
| 15~8 | PAB5 | physical address byte 5 | From EEPROM | R/W |
| 7~0 | PAB4 | physical address byte 4 | From EEPROM | R/W |

for example, physical address = 00-00-e8-11-22-33

PAR0= 11 e8 00 00

PAR1= xx xx 33 22

PAR0 and PAR1 are readable, but can be written only if the receive state is in stopped state (CSR5 bit19-17=000).

CSR27 (offset = ach) - MAR0, multicast address hash table register 0

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~24 | MAB3 | multicast address byte 3 (hash table 31:24) | 0 | R/W |
| 23~16 | MAB2 | multicast address byte 2 (hash table 23:16) | 0 | R/W |
| 15~8 | MAB1 | multicast address byte 1 (hash table 15:8) | 0 | R/W |
| 7~0 | MAB0 | multicast address byte 0 (hash table 7:0) | 0 | R/W |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****CSR28 (offset = b0h) - MAR1, multicast address hash table register 1**

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|---|-------------|---------|
| 31~24 | MAB7 | multicast address byte 7 (hash table 63:56) | 0 | R/W |
| 23~16 | MAB6 | multicast address byte 6 (hash table 55:48) | 0 | R/W |
| 15~8 | MAB5 | multicast address byte 5 (hash table 47:40) | 0 | R/W |
| 7~0 | MAB4 | multicast address byte 4 (hash table 39:32) | 0 | R/W |

MAR0 and MAR1 are readable, but can be written only if the receive state is in stopped state (CSR5 bit19-17=000).

CSR29 (offset = b4h) – MDMCTL, Modem control register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|----------|--|---------------------|---------|
| 31 | MDM | Modem function enable 1: enable the modem interface. The modem pins are shared with boot ROM interface. By setting this pin, the shared pins will be output as modem pins. 0: disable modem interface. | 1 from EEPROM | R/W |
| 30 | --- | Reserved, must be set to 0 | 0 | |
| 29 | BROM_DIS | Boot ROM disable 1: disable Boot ROM detection on PCI configuration 0: enable Boot ROM detection on PCI configuration | 0 from EEPROM | R/W |
| 28 | --- | Reserved, must be set to 1 | 1 | |
| 27 | INT_sel | Reserved. | 0 | |
| 26 | RING_sel | Select the polarity of RING output 1 : RING asserts an active low signal 0 : RING asserts an active high signal | 1 from EEPROM | R/W |
| 25-0 | | Reserved | 0 | |

CSR30 (offset = fch) – MCMR, Misc controller mode register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------|---|-------------|---------|
| 31 | SPEED | Network Speed Status 1: 100M 0: 10M | 0 | RO |
| 30 | FD | Full/Half Duplex Status 1: Full duplex 0: Half duplex | 0 | RO |
| 29 | LINK | Network Link Status 1: Link On 2: Link Off | 0 | RO |

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| | | | | |
|-------|----------|---|------|-----|
| 28~27 | Reserved | | 0 | |
| 26 | EERLOD | Write 1 to this bit will cause ADM9511 to reload data from EEPROM. After reload completed, this bit will be cleared automatically. | 0 | R/W |
| 25~3 | Reserved | | 0 | |
| 2~0 | OpMode | <p>These three bits are used to configure ADM9511's operation mode:</p> <p>111b: Single Chip mode (Normal operation) At this mode, ADM9511 is configured as single chip to provide PCI to Ethernet controller.</p> <p>100b: MAC-only mode The ADM9511 is configured as a MAC only controller, it provides standard MII interface to link to the external PHY. This mode can support HomePNA application.</p> <p>Others: For diagnostic purpose.</p> | 111b | R/W |

CSR31 (offset = 100h) – FER, Function event register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------------|---|-------------|---------|
| 31~16 | Reserved | | 0 | |
| 15 | INTR_EVENT | This bit is used as the interrupt bit. It is set when the Ethernet interrupt source is set, regardless of the mask value. It is cleared when the OS writes 1b to this field and the interrupt source has been serviced. Writing 0b to this field has no effect. | 0 | R/W1C* |
| 14~5 | Reserved | | 0 | |
| 4 | GWAKE_EVENT | This bit is used for general wake-up. It is set when the Ethernet wake-up source is set, regardless of the mask value. Writing 1b to this field clears this bit and the PME Status bit in the PMCSR. Writing 0b to this field has no effect. Note that writing 1b to the PME Status bit in the PMCSR has the same effect. | 0 | R/W1C |
| 3~0 | Reserved | | 0 | |

CSR32 (offset = 104h) – FEMR, Function Event Mask Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--------------|-------------|---------|
|-------|------|--------------|-------------|---------|

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| | | | | |
|-------|----------|---|---|-----|
| 31~16 | Reserved | | 0 | |
| 15 | INTR_EN | The bit is the interrupt mask. When this bit equals 0b, it masks the Ethernet function INTA# line but has no effect on the Function Event register. The interrupt mask bit affects the INTA# masking. | 1 | R/W |
| 14 | WKUP_EN | This bit is the wake-up mask. When this bit equals 0b, it masks the Ethernet function CSTSCHG signal but has no effect on the Function Event register. This bit is dependent on bit 4 of this register. | 0 | R/W |
| 13~5 | Reserved | | 0 | |
| 4 | GWAKE_EN | This bit is the general wake-up mask. When this bit equals 0b, it masks the Ethernet function wake-up events towards the CSTSCHG signal. It has no effect on the Function Event register. The ADM9511 can assert the CSTSCHG signal in the following configuration of masked bits: wake-up bit AND general wake-up bit, or PME Enable bit in the PMCSR register only. | 0 | R/W |
| 3~0 | Reserved | | 0 | |

CSR33 (offset = 108h) – FPSR, Function present state register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------------------|--|-------------|---------|
| 31~16 | Reserved | | 0 | |
| 15 | INTR_ST ATUS | This bit is used for interrupts. It reflects the current state of the Ethernet source of the interrupt regardless of the mask value. It is set when the Ethernet function has a pending interrupt and cleared when the software driver acknowledges all active interrupts through the SCB Command Word. | 0 | RO |
| 14~5 | Reserved | | 0 | |
| 4 | WAKEUP _STATUS | This bit is used for general wake-up. It reflects the current state of the Ethernet source of CSTSCHG. It is a logical OR result of the gated three most significant bits in the PMDR: Link Status change bit is gated by the Link Status Change Wake Enable bit in the Configuration command. The Magic Packet bit is gated by the Magic Packet Wake-up disable bit in the Configuration command. The Interesting Packet bit is gated by the programmable filter command. | 0 | RO |
| 3~0 | Reserved | | | |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****CSR34 (offset = 10ch) – FFER, Function force event register**

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-----------------|---|-------------|---------|
| 31~16 | Reserved | | 0 | |
| 15 | INTA_FO RCE | This bit is used for interrupts. Writing 1b in this field will set the interrupt bit in the Function Event register. If the INTA# pin is not masked, then it will also be activate. Writing 0b has no effect. | 0 | R/W1S |
| 14~5 | Reserved | | 0 | |
| 4 | GWAKE_ FORCE | This bit is used for general wake-up. Writing 1b in this field will set the CSTSCHG bit in the Function Event register. If the CSTSCHG pin is not masked, then it will also be activated. Writing 0b has no effect. | 0 | R/W1S |
| 3~0 | Reserved | | | |

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8.2.2. Modem Control/Status registers

The base address of Modem Control/Status registers are specified in Function 1 PCI configuration registers. The registers occupy eight words of I/O, or memory mapped I/O, address space in the PCI allocated resource. Through these eight base I/O spaces, an index addressing method is used to extend the register space beyond eight words.

All PCT HSP registers are arranged in 16-bit format, each one is accessibly by writing to INDEX register first with the appropriate index address then read or write to the addressed register via DATA port. The index range allocated for on-chip registers is from index 0 through 15.

| offset from base address | Length | Name | Descriptions |
|--------------------------|-----------|-------|-------------------------------------|
| 00h | 2 bytes | DATA | Data Register |
| 02h | 2 bytes | INDEX | Index Register |
| 04h | 2 bytes | --- | Reserved |
| 06h | 2 bytes | --- | Reserved |
| 08h | 2 bytes | --- | Reserved |
| 0Ah | 2 bytes | --- | Reserved |
| 0Ch | 2 bytes | --- | Reserved |
| 0Eh | 2 bytes | --- | Reserved |
| F0h | 4 bytes | MFER | Modem function event register |
| F4h | 4 bytes | MFMR | Modem function mask register |
| F8h | 4 bytes | MFPR | Modem function present register |
| FCh | 4 bytes | MFFER | Modem force function event register |
| 100h~1FFh | 256 bytes | | Modem CIS area (load from EEPROM) |

8.2.2.1. Modem Control/Status registers description

DATA (offset = 00h) – Data register.

This Base I/O location is the 16-bit data port for the host to communicate with PCT HSP control/status registers.

INDEX (offset = 02h)

This Base I/O location is write-only, it is used as the address register for all PCT HSP registers

MFER (offset = F0h) – Modem function event register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|----------|--------------|-------------|---------|
| 31~16 | Reserved | | 0 | |

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| | | | | |
|------|-----------------|--|---|--------------|
| 15 | INTR_EV ENT | This bit is used for as the interrupt bit. It is set when the internal modem interrupt occurred, regardless of the mask value. It is cleared when the OS writes 1b to this field and the interrupt source has been serviced. Writing 0b to this field has no effect. | 0 | RLH*/W 1C |
| 14~5 | Reserved | | 0 | |
| 4 | GWAKE_ EVENT | This bit is used for general wake-up. It is set when the RING pin is asserted, regardless of the mask value. Writing 1b to this field clears this bit. Writing 0 to this field has no effect. | 0 | R/W1C |
| 3~0 | Reserved | | 0 | |

MFMR (offset = F4h) – Modem function event mask register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|--------------|--|-------------|---------|
| 31~16 | Reserved | | 0 | |
| 15 | INTR_EN | The bit is the interrupt mask. When this bit equals 0b, it masks the internal modem interrupt function INTA# line but has no effect on the Function Event register. The interrupt mask bit affects the INTA# masking. | 1 | R/W |
| 14 | WKUP_E N | This bit is the wake-up mask. When this bit equals 0b, it masks the CSTSCHG signal but has no effect on the Function Event register. This bit is dependent on bit 4 of this register. | 0 | R/W |
| 13~5 | Reserved | | 0 | |
| 4 | GWAKE_ EN | This bit is the general wake-up mask. When this bit equals 0b, it masks the RING pin wake-up events towards the CSTSCHG signal. It has no effect on the Function Event register. The ADM9511 can assert the CSTSCHG signal in the following configuration of masked bits: wake-up bit AND general wake-up bit, or PME Enable bit in the PMCSR register only. | 0 | R/W |
| 3~0 | Reserved | | 0 | |

MFPR (offset = F8h) – Modem function present state register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-----------------|---|-------------|---------|
| 31~16 | Reserved | | 0 | |
| 15 | INTR_ST ATUS | This bit is used for interrupts. It reflects the current state of the internal modem interrupt status regardless of the mask value. It is set when the internal modem interrupt has a pending interrupt and cleared when the software driver acknowledges all active interrupts | 0 | RO |
| 14~5 | Reserved | | 0 | |
| 4 | WAKEUP | This bit is used for general wake-up. It reflects the current | 0 | RO |

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| | | | | |
|-----|----------|--|---|--|
| | _STATUS | state of the RING status from the modem. | | |
| 3~0 | Reserved | | 0 | |

MFFER (offset = FCh) – Modem function force event register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------------|---|-------------|---------|
| 31~16 | Reserved | | | |
| 15 | INTA_FORCE | This bit is used for interrupts. Writing 1b in this field will set the interrupt bit in the Function Event register. If the INTA# pin is not masked, then it will also be activate. Writing 0b has no effect. | 0 | W |
| 14~5 | Reserved | | | |
| 4 | GWAKE_FORCE | This bit is used for general wake-up. Writing 1b in this field will set the CSTSCHG bit in the Function Event register. If the CSTSCHG pin is not masked, then it will also be activated. Writing 0b has no effect. | 0 | W |
| 3~0 | Reserved | | | |

8.2.2.2. PCT HSP control registers description**PCT HSP registers list**

| INDEX | WRITE | | READ | |
|-------|--------------|-----------|--------------|--------------|
| | Hi Byte | Lo Byte | Hi Byte | Lo Byte |
| 0 | TxData[15:0] | | RxData[15:0] | |
| 1 | CNTL[15:0] | | STS[15:0] | |
| 2 | MASK[1:0] | OBIO[1:0] | Reserved | EXTIN[7:0] |
| 3 | Reserved | TOC[3:0] | Reserved | ERRCNT[11:0] |
| 4 | Reserved | Reserved | Reserved | Reserved |
| 5 | Reserved | Reserved | Reserved | CLK1D[7:0] |
| 6 | Reserved | Reserved | Reserved | VIDWE[7:0] |
| 7 | Reserved | Reserved | Reserved | Reserved |

TxData[15:0] : Transmit Data Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------------|---|-------------|---------|
| 15~0 | TxData[15..0] | Transmit data register is the input port to the transmit FIFO | | W |

RxData[15:0] : Receive Data Register**ADMtek Inc.**1F, No9, Industrial E. 9th Road

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| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------------|--|-------------|---------|
| 15~0 | RxData[15..0] | Receive data register is the output port from the receive FIFO | 0 | R |

CNTL[15:0] : Control Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|--------|---------------------------------|-------------|---------|
| 15 | SLEEP | Power-down ADM9511 | | W |
| 14~12 | ... | Reserved | | |
| 11 | AFERST | AFE Reset (active low) | | W |
| 10~9 | ... | Reserved | | |
| 8 | LPBMD0 | Loop-back test | | W |
| 7 | NTORST | Disable Time-out Reset (level) | | W |
| 6 | ENIRQ | IRQ Enable (level) | | W |
| 5 | START | Start (positive-edge) | | W |
| 4 | ... | Reserved | | |
| 3 | ENTX | Transmit enable (positive-edge) | | W |
| 2~0 | ... | Reserved | | |

STS[15:0] : Status Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------|---------------------------------------|-------------|---------|
| 15~3 | ... | Reserved | | |
| 2 | IRQS | IRQS (reset after read) | | R |
| 1 | RxOVRUN | Rx buffer overrun (reset after read) | | R |
| 0 | TxUDRUN | Tx buffer underrun (reset after read) | | R |

EXTOUT[15:0] : External Output Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------------|------------------------|-------------|---------|
| 15~14 | ... | Reserved | | |
| 13~12 | MASK[1..0] | GPIO direction control | 11b | W |
| 11~10 | ... | Reserved | | |
| 9~8 | OBIO[1..0] | GPIO input register | 00b | W |
| 7~1 | ... | Reserved | | |
| 0 | EXTOUT0 | Off-Hook Relay control | | W |

EXTIN[15:0] : External Input Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------|--------------|-------------|---------|
| 15~6 | ... | Reserved | | |

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| | | | | |
|-----|------------|----------------------|--|---|
| 5~4 | IBIO[1..0] | GPIO output register | | R |
| 3~1 | ... | Reserved | | |
| 0 | EXTIN0 | Ring detect input | | R |

Miscellaneous Control Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|------------|---|-------------|---------|
| 15 | RINGEN | PME# Wake on Ring Enable allows the Ring detect input to drive PCI bus PME# signal for wake-on-ring event. (sticky) | | W |
| 14~12 | ... | Reserved | | |
| 11~8 | TOC[3..0] | Time-out Count Register allows the ADM9511 to generate internal time-out if errors detected for (N+1)*256*3.3ms, where N=0~15. | 0 | W |
| 7~0 | FFSZ[7..0] | FIFO size Control Register allows Tx and Rx buffer size to be chosen up to 128 words deep (the legal number accepted is between 16 and 128). Whenever the Rx buffer is full, a pre-selected IRQ is generated, if enabled. | 20h | W |

ERRCNT[15:0] : Error Count Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------------|--|-------------|---------|
| 15~12 | ... | Reserved | | |
| 11~0 | ERRCNT[11..0] | Error Count records the number of overrun and underrun errors occurred | 0 | R |

CLK1D[7:0] : MCLK Divider Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|-------------|---|-------------|---------|
| 15~8 | ... | Reserved | | |
| 7~0 | CLK1D[7..0] | MCLK Divider Register, provides a programmable divider for generating MCLK output for various CODEC from the X'tal oscillator input. Bit 7-6: 00 - *2 invert 01 - *2 10 - /1 11 - /2 Bit 5-3: 000 - DIVA =1 001 - DIVA = 2 010 - DIVA = 3 011 - DIVA =4 100 - DIVA = 5 101 - DIVA = 6 110 - Reserved | 80h | R/W |

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| | | 111 - DIVA = 8 Bit 2-0: 000 - DIVB=1 001 - DIVB=2.5 010 - DIVB=3 011 - DIVB=3.5 100 - DIVB=4 101 - DIVB=4.5 110 - DIVB=5 111 - DIVB=5.5 | | |
|--|--|---|--|--|

VIDWE[7:0] : Subsystem ID Write Enable Control Register

| Bit # | Name | Descriptions | Default Val | RW Type |
|-------|---------|---|-------------|---------|
| 15~3 | ... | Reserved | | |
| 2 | CKRUNEN | CLKRUN Enable allows SW to turn on or off CLKRUN control, when it is enabled, it allows PCI clock to be shut off by the system chip set when necessary. Otherwise, it drives CLKRUN active to prohibit the system PCI clock shut off request. | | R/W |
| 1 | SYIDWEN | Subsystem ID Write Enable allows BIOS to write into Subsystem ID register in PCI Configuration register area | | R/W |
| 0 | SVIDWEN | Subsystem Vender ID Write Enable allows BIOS to write into Subsystem Vendor ID register in PCI Configuration register area. | | R/W |

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8.3. Transceiver (XCVR) Registers

The Transceiver registers are accessed from CSR9 MDI/MMC/MDO/MDC

8.3.1. Transceiver registers list

| Register | Description | Default |
|-----------------|--|----------------|
| 0 | Control Register | 1000 |
| 1 | Status Register | 7849 |
| 2 | PHY Identifier 1 Register | 0022 |
| 3 | PHY Identifier 2 Register | 5513 |
| 4 | Auto-Negotiation Advertisement Register | 01E1 |
| 5 | Auto-Negotiation Link Partner Ability Register | 0001 |
| 6 | Auto-Negotiation Expansion Register | 0004 |
| 7 | Next Page Advertisement Register | 2001 |
| 8-15 | Reserved | XXXX |
| 16 | TDK specific Register | 0540 |
| 17 | Interrupt Control/Status Register | 0000 |
| 18 | Diagnostic Register | 0000 |
| 19 | Power Management & Loopback Register | 0020 |
| 20 | Loopback and Power management Register | XXFX |
| 21 | Mode Control Register | 0304 |
| 22 | Reserved | XXXX |
| 23 | PLL Lock Register | 0000 |
| 24 | Receive Error Counter Register | 0000 |
| 25-31 | Reserved | XXXX |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****8.3.2. Transceiver registers description**

Legend:

| Type | Description | Type | Description |
|------|-----------------------|------|-------------------------------|
| RW | Readable and writable | RO | Read Only |
| SC | Self Clearing | RC | Cleared on the read operation |
| LL | Latch Low until clear | LH | Latch high until clear |

Register 0: Control Register

| Reg.bit | Name | Description | Mode | Default |
|---------|--------------------------|--|-------|---------|
| 0.15 | Reset | 1 = PHY reset. This bit is self-clearing. | RW/SC | 0 |
| 0.14 | Loopback | 1 = Enable loopback mode. This will loopback TXD to RXD, thus it will ignore all the activity on the cable media. 0 = Normal operation. | RW | 0 |
| 0.13 | Speed Select | 1 = 100Mbps, 0 = 10Mbps. This bit will be ignored if Auto Negotiation is enabled (0.12=1). | RW | 1 |
| 0.12 | Auto-Neg. Enable | 1 = Enable auto-negotiate process (overrides 0.13 and 0.8) 0 = Disable auto-negotiate process. | RW | 1 |
| 0.11 | Power Down | 1 = Power down. ADM9511 will shut off all blocks except for MDIO/MDC interface. 0 = Normal operation. | RW | 0 |
| 0.10 | Isolate | 1 = Electrically isolate the PHY from MII. However, PHY is still able to response to MDC/MDIO. 0 = Normal operation. | RW | 0 |
| 0.9 | Restart Auto-Negotiation | 1 = Restart Auto-Negotiation process. 0 = Normal operation. | RW/SC | 0 |
| 0.8 | Duplex Mode | 1 = Full duplex. 0 = Half duplex. If Auto-Neg. enabled: This bit is writable but will be ignored. | RW | 0 |
| 0.7 | Collision Test | 1 = Enable collision test, which issues the COL signal in response to the assertion of TX_EN signal. 0 = disable COL test. | RW | 0 |
| 0.[6:0] | Reserved | | RW | 0000000 |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****Register 1: Status Register**

| Reg.bit | Name | Description | Mode | Default |
|----------|-------------------------------|--|-------|---------|
| 1.15 | 100Base-T4 | Permanently tied to zero indicates no 100BaseT4 capability. | RO | 0 |
| 1.14 | 100Base-T X Full Duplex | 1 = 100BaseTX with full duplex. 0 = No 100BaseTX full duplex ability. | RO | 1 |
| 1.13 | 100Base-T X Half Duplex | 1 = 100BaseTX with half duplex. 0 = No TX half-duplex ability. | RO | 1 |
| 1.12 | 10Base-T Full Duplex | 1 = 10BaseT with full duplex. 0 = No 10BaseT full duplex ability. | RO | 1 |
| 1.11 | 10Base-T Half Duplex | 1 = 10BaseT with half duplex. 0 = No 10BaseT half-duplex ability. | RO | 1 |
| 1.[10:6] | Reserved | | RO | 00000 |
| 1.5 | Auto-Negotiate Complete | 1 = Auto-negotiate process completed. Reg. 4, 5, 6 are valid after this bit is set. 0 = Auto-negotiate process not completed. | RO | 0 |
| 1.4 | Remote Fault | 1 = Remote fault condition detected. 0 = No remote fault. This bit will remain set until it is cleared by reading register 1 via management interface. | RO/LH | 0 |
| 1.3 | Auto-Negotiate Ability | 1 = Able to perform Auto-Negotiation function, its value is determined by ANEGA pin. 0 = Unable to perform Auto-Negotiation function. | RO | 1 |
| 1.2 | Link Status | 1 = Link is established. This is Latched bit. Therefore, if ADM9511 link failed, this bit will be cleared and remain "0" until register is read again via management interface. 0 = link is down. | RO/LL | 0 |
| 1.1 | Jabber Detect | 1 = Jabber condition detect. 0 = No Jabber condition detected. | RO/LH | 0 |
| 1.0 | Extended Capability | 1 = Extended register capable. This bit is tied permanently to one. | RO | 1 |

Register 2: PHY Identifier 1 Register

| Reg.bit | Name | Description | Mode | Default |
|----------|------|--|------|---------|
| 2.[15:0] | OUI | Composed of the 3rd through 18th bits of the Organizationally Unique Identifier (OUI), respectively. | RO | 0382(H) |

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****Register 3: PHY Identifier 2 Register**

| Reg.bit | Name | Description | Mode | Default |
|-----------|-----------------|--|------|---------|
| 3.[15:10] | OUI | Assigned to the 19th through 24th bits of the OUI. | RO | 010010 |
| 3.[9:4] | Model Number | Six bit manufacturer's model number. | RO | 000001 |
| 3.[3:0] | Revision Number | Four-bit manufacturer's revision number. | RO | 0000 |

Register 4: Auto-Negotiation Advertisement Register

| Reg.bit | Name | Description | Mode | Default |
|-----------|------------------------|--|------|---------|
| 4.15 | Next Page | 1 = Next Page enabled. 0 = Next Page disabled. | RW | 0 |
| 4.14 | Acknowledge | This bit will be set internally after receiving 3 consecutive and consistent FLP bursts. | RO | 0 |
| 4.13 | Remote Fault | 1 = Advertises that this device has detected a Remote Fault. 0 = No remote fault detected. | RW | 0 |
| 4.[12:10] | Reserved | For future technology. | RW | 000 |
| 4.9 | 100Base-T4 | ADM9511 doesn't support 100BaseT4 function, i.e., this bit ties to zero. | RO | 0 |
| 4.8 | 100Base-TX Full Duplex | 1 = 100BaseTX full duplex supported by Local device. 0 = 100BaseTX full duplex not supported by Local device. Default is set by Reg. 1.14. | RW | 1 |
| 4.7 | 100Base-TX | 1 = 100BaseTX supported by Local device. 0 = 100BaseTX not supported by Local device. Default is set by Reg. 1.13. | RW | 1 |
| 4.6 | 10Base-T Full Duplex | 1 = 10Mbps full duplex supported by Local device. 0 = 10Mbps full duplex not supported by Local device. Default is set by Reg. 1.12. | RW | 1 |
| 4.5 | 10Base-T | 1 = 10Mbps supported by Local device. 0 = 10Mbps not supported by Local device. Default is set by Reg. 1.11. | RW | 1 |
| 4.[4:0] | Selector Field | Protocol Selection [00001] = IEEE 802.3. | RW | 00001 |

Register 5: Auto-Negotiation Link Partner Ability Register

| Reg.bit | Name | Description | Mode | Default |
|---------|------|-------------|------|---------|
|---------|------|-------------|------|---------|

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| | | | | |
|-----------|------------------------|--|----|-------|
| 5.15 | Next Page | 1 = Link partner desires Next Page transfer. 0 = Link partner does not desire Next Page transfer. | RO | 0 |
| 5.14 | Acknowledge | 1 = Link Partner acknowledges reception of FLP words. 0 = No acknowledged by Link Partner. | RO | 0 |
| 5.13 | Remote Fault | 1 = Remote Fault indicated by Link Partner. 0 = No remote fault detected by Link Partner. | RO | 0 |
| 5.[12:10] | Reserved | For future technology. | RO | 000 |
| 5.9 | 100Base-T4 | 1 = 100BaseT4 supported by Link Partner. 0 = 100BaseT4 not supported by Link Partner. | RO | 0 |
| 5.8 | 100Base-TX Full Duplex | 1 = 100BaseTX full duplex supported by Link Partner. 0 = 100BaseTX full duplex not supported by Link Partner. | RO | 0 |
| 5.7 | 100Base-TX | 1 = 100BaseTX supported by Link Partner. 0 = 100BaseTX not supported by Link Partner. | RO | 0 |
| 5.6 | 10Base-T Full Duplex | 1 = 10Mbps full duplex supported by Link Partner. 0 = 10Mbps full duplex not supported by Link Partner. | RO | 0 |
| 5.5 | 10Base-T | 1 = 10Mbps supported by Link Partner. 0 = 10Mbps not supported by Link Partner. | RO | 0 |
| 5.[4:0] | Selector Field | Protocol Selection [00001] = IEEE 802.3. | RO | 00001 |

Register 6: Auto Negotiation Expansion Register

| Reg.bit | Name | Description | Mode | Default |
|----------|-----------------------------|---|-------|---------|
| 6.[15:5] | Reserved | | RO | 0 |
| 6.4 | Parallel Detection Fault | 1 = Fault detected by parallel detection logic, this fault is due to more than one technology detecting concurrent link up condition. This bit can be only cleared by reading this register using the management interface. 0 = No fault detected by parallel detection logic. | RO/LH | 0 |
| 6.3 | Link Partner Next Page Able | 1 = Link partner support next page function. 0 = Link partner does not support next page function. | RO | 0 |
| 6.2 | Next Page Able | Next page is supported, i.e., this bit is permanently ties to 1. | RO | 1 |
| 6.1 | Page Received | It is set when a new link code word has been received into the Auto-Negotiation Link Partner Ability Register. This bit is cleared upon a read of this register. | RO | 0 |
| 6.0 | Link | 1 = Link partner is Auto-Negotiation capable. | RO | 0 |

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| Reg.bit | Name | Description | Mode | Default |
|---------|-------------------------------|---|------|---------|
| | Partner Auto-Negotiation Able | 0 = Link partner is not Auto-Negotiation capable. | | |

Register 7: Auto Negotiation Next Page Transmit Register (ANNPTR)

| Reg.bit | Name | Description | Mode | Default |
|-----------|----------|---|------|---------|
| 7.15 | NP | Next page indication: 1 = Another Next Page desired. 0 = No other Next Page Transfer desired. | RW | 0 |
| 7.14 | Reserved | - | RO | 0 |
| 7.13 | MP | Message page: 1 = Message page. 0 = Un-formatted page. | RW | 1 |
| 7.12 | ACK2 | Acknowledge 2 1 = Will comply with message. 0 = Can not comply with message. | RW | 0 |
| 7.11 | TOG_TX | Toggle: 1 = Previous value of transmitted link code word equals to 0. 0 = Previous value of transmitted link code word equals to 1. | RW | 0 |
| 17.[10:0] | CODE | Message/Un-formatted Code Field. | RW | 001 |

Register 16: ADM9511 Specific Register

| Reg.bit | Name | Description | Mode | Default |
|------------|------------------|--|------|-------------|
| 16.15 | Repeater | 1 = Repeater mode, full-duplex will be inactive, and CRS only responses to receive activity. SQE test function is also disabled. | RW | Set by RPTR |
| 16.14 | INTR_LE VL | INTR pin will be active high if this register bit is set to 1. INTR pin will be active low if this register bit is set to 0. | RW | 0 |
| 16.[13:12] | Reserved | | RW | 00 |
| 16.11 | SQE Test Inhibit | 1 = Disable 10BaseT SQE testing. 0 = Enable 10BaseT SQE testing, which will generate a COL pulse following the completion of a packet transmission. | RW | 0 |
| 16.10 | 10BaseT Loopback | 1 = Enable normal loopback in 10BaseT mode. 0 = Disable normal loopback in 10BaseT mode. | RW | 1 |
| 16.[9:6] | Reserved | . | RO | 0000 |
| 16.5 | Auto | 1 = Disable auto polarity detection / correction. | RW | 0 |

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| Reg.bit | Name | Description | Mode | Default |
|----------|-----------------------|--|------|---------|
| | polarity Disable | 0 = Enable auto polarity detection / correction. | | |
| 16.4 | Reverse Polarity | If Reg. 16.5 is set to 0, and Reverse polarity is detected on the media, this bit will get set to 1. If Reg. 16.5 is set to 1, writing a one to this bit will reverse the polarity of the transmitter. Note: the reverse polarity is detected either through 8 inverted NLPs or through a burst of inverted FLP. | RW | 0 |
| 16.[3:1] | Reserved | | RO | 000 |
| 16.0 | Receive Clock Control | Write a one to this bit will shut off RX_CLK when incoming data is not present. RX_CLK will resume active 1 clock cycle prior to RX_DV goes high, and shut off 64 clock cycles after RX_DV goes low. However, in loopback and PCS bypassed modes, writing to this bit does not affect RX_CLK. Receive clock will be active all the time. | RW | 0 |

Register 17: Interrupt Control/Status Register

| Reg.bit | Name | Description | Mode | Default |
|---------|----------------|--|------|---------|
| 17.15 | Jabber IE | Jabber Interrupt Enable. | RW | 0 |
| 17.14 | Rx Er IE | Receive Error Interrupt Enable. | RW | 0 |
| 17.13 | Page Rx IE | Page Received Interrupt Enable. | RW | 0 |
| 17.12 | PD Fault IE | Parallel Detection Fault Interrupt Enable. | RW | 0 |
| 17.11 | LP Ack IE | Link Partner Acknowledge Interrupt Enable. | RW | 0 |
| 17.10 | Link Not OK IE | Link Status Not OK Interrupt Enable. | RW | 0 |
| 17.9 | R Fault IE | Remote Fault Interrupt Enable. | RW | 0 |
| 17.8 | ANeg Comp IE | Auto-Negotiation Complete Interrupt Enable. | RW | 0 |
| 17.7 | Jabber Int | This bit is set when a jabber event is detected. | RC | 0 |
| 17.6 | Rx Er Int | This bit is set when RX_ER transitions high. | RC | 0 |
| 17.5 | Page Rx Int | This bit is set when a new page is received from link partner during Auto-Neg. | RC | 0 |
| 17.4 | PD Fault Int | This bit is set when parallel detect fault is detected. | RC | 0 |
| 17.3 | LP Ack Int | This bit is set when the FLP with acknowledge bit set is received. | RC | 0 |
| 17.2 | Link Not | This bit is set when link status switches from OK | RC | 0 |

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| | OK Int | status to Non-OK status (Fail or Ready). | | |
| 17.1 | R_Fault_In t | This bit is set when remote fault is detected. | RC | 0 |
| 17.0 | A_Neg_Co mp Int | This bit is set when Auto-Neg is complete. | RC | 0 |

* See Interrupt Source Table for bit assignments

Register 18: Diagnostic Register

| Reg.bit | Name | Description | Mode | Default |
|------------|----------|---|-------|---------|
| 18.[15:12] | Reserved | | RO | 0000 |
| 18.11 | DPLX | This bit indicates the result of the Auto-Neg for duplex arbitration. | RO | 0 |
| 18.10 | Speed | This bit indicates the result of the Auto-Neg for data speed arbitration. | RO | 0 |
| 18.9 | RX_PASS | In 10BT mode, this bit indicates that Manchester data has been detected. In 100BT mode, it indicates valid signal has been received but not necessarily locked on to. | RO | 0 |
| 18.8 | RX_LOCK | Indicates the receive PLL has locked onto the received signal for the selected speed of operation (10Base-T or 100Base-TX). This bit is set whenever a cycle-slip occurs, and will remain set until it is read. | RO/SC | 0 |
| 18.[7:0] | Reserved | | RO | 0 |

Register 19: Power/Loopback Register

| Reg.bit | Name | Description | Mode | Default |
|-----------|-----------------------|--|------|---------|
| 19.[14:7] | Reserved | | RW | 00 |
| 19.6 | TP125 | Transmit transformer ratio selection 1 = 1.25:1 0 = 1:1 | RW | 0 |
| 19.5 | Low Power Mode | 1 = Enable advanced power saving mode. 0 = Disable advanced power saving mode. | RW | 1 |
| 19.4 | Test Loopback | 1 = Enable test loopback. Data will be transmitted from MII interface to clock recovery and loopback to MII received data. | RW | 0 |
| 19.3 | Digital loopback | 1 = Enable loopback. 0 = Normal operation. | RW | 0 |
| 19.2 | LP_LPBK | 1 = Enable link pulse loopback. 0 = Normal operation. | RW | 0 |
| 19.1 | NLP Link Integrity | 1 = In Auto-Neg test mode, send NLP instead of FLP in order to test NLP receive integrity. | RW | 0 |

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|------|--------------|--|---|---|
| | Test | 0 = Sending FLP in Auto-Neg test mode. | | |
| 19.0 | Reduce Timer | 1= Reduce time constant for Auto-Negotiation timer. 0 = Normal operation. | R | 0 |

Register 20: Loopback and Power Management Register

| Reg.bit | Name | Description | Mode | Default |
|-----------|------------------------------|---|------|---------|
| 20.[15:8] | Reserved | | RO | 0 |
| 20.[7:4] | Cable measurement capability | These bits can be used as cable length indicator. The bits are incremented from 0000 to 1111, with an increment of approximately 10 meters. The equivalent is 0 to 32 dB with an increment of 2 dB @ 100MHz. The value is a read back from the equalizer, and the measured value is not absolute. | RO | 0 |
| 20.[3:0] | Reserved | | RO | 0 |

Register 21: Mode Control Register

| Reg.bit | Name | Description | Mode | Default |
|-----------|--------------------|---|--------|--------------------------------|
| 21.15 | Reserved | | RO | 0 |
| 21.14 | NLP Disable | 1 = Force 10B-T link up without checking NLP. 0 = Normal Operation. | RW | 0 |
| 21.13 | Force_link_up | 1 = force link up , auto negotiation must be disabled at this time | R/W | 0 |
| 21.12 | Jabber Disable | 1 = Disable Jabber function in PHY. 0 = Enable Jabber function in PHY. | RW | 0 |
| 21.11 | 10BT_Sel | 1 = Enable 7-wire interface for 10Base-T operation. This bit is useful only when the chip is not in PCS bypass mode. 0 = Normal operation. | RW | 0 |
| 21.[10:9] | Reserved | | RO | 0 |
| 21.8 | FEF_Disable | 1 = Enable far-end-fault generation and detection function. 0 = Disable far-end-fault. | RW | Set by TECH FX_SEL ANEGA |
| 21.7 | Force FEF Transmit | This bit is set to force to transmit Far End Fault (FEF) pattern. | RW | 0 |
| 21.6 | Rx_Er_Cnt_Full | When Receive Error Counter is full, this bit will get set to one. | RO/ RC | 0 |
| 21.5 | Disable Rx_Er_Cnt | 1 = Disable Receive Error Counter. 0 = Enable Receive Error Counter. | RW | 0 |
| 21.4 | Dis_WDT | 1 = Disable the watchdog timer in the decipher. 0 = Enable watchdog timer. | RW | 0 |

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| Reg.bit | Name | Description | Mode | Default |
|----------|----------|--|------|---------|
| 21.3 | En_RPBK | 1 = Enable remote loopback. 0 = Disable remote loopback. | RW | 0 |
| 21.2 | Dis_Scrm | 1 = Enable data scrambling. 0 = Disable data scrambling. When FX mode is selected, this bit will be forced to one. | RW | 1 |
| 21.[1:0] | Reserved | | RO | |

Register 23: PLL Lock Register

| Reg.bit | Name | Description | Mode | Default |
|-----------|--------------------|-----------------------------|------|---------|
| 23.[15:0] | DLOCK drop counter | Count PLL lock drop events. | RW | 0000 |

Register 24: Receive Error Counter Register

| Reg.bit | Name | Description | Mode | Default |
|-----------|---------------|-----------------------------|------|---------|
| 24.[15:0] | RX_ER counter | Count receive error events. | RW | 0000 |

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8.4.Descriptors and Buffer Management

The ADM9511 provides receive and transmit descriptors for packet buffering and management.

8.4.1. Receive descriptor

8.4.1.1. Receive descriptor table

| | | | | |
|-------|-------------------------------|--------|---------|--------------------|
| | 31 | | | 0 |
| RDES0 | Own | Status | | |
| RDES1 | | --- | Control | Buffer2 byte-count |
| RDES2 | Buffer1 address (DW boundary) | | | |
| RDES3 | Buffer2 address (DW boundary) | | | |

Descriptors and receive buffers addresses must be double word alignment

8.4.1.2. Receive descriptor description

RDES0

| Bit # | Name | Descriptions |
|-------|------|--|
| 31 | OWN | Own bit 1: indicate the new receiving data can be put into this descriptor 0: Host does not move the receiving data out yet. |
| 30-16 | FL | Frame length, including CRC. This field is valid only in last descriptor |
| 15 | ES | Error summary, OR of the following bit 0: overflow 1: CRC error 6: late collision 7: frame too long 11: runt packet 14: descriptor error This field is valid only in last descriptor. |
| 14 | DE | Descriptor error. This bit is valid only in last descriptor 1: the current receiving packet is not able to put into the current valid descriptor. This packet is truncated. |
| 13-12 | DT | Data type. 00: normal 01: MAC loop-back 10: Transceiver loop-back 11: remote loop-back These bits are valid only in last descriptor |

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| | | |
|----|----------|---|
| 11 | RF | Runt frame (packet length < 64 bytes). This bit is valid only in last descriptor |
| 10 | MF | Multicast frame. This bit is valid only in last descriptor |
| 9 | FS | First descriptor. |
| 8 | LS | Last descriptor. |
| 7 | TL | Too long packet (packet length > 1518 bytes). This bit is valid only in last descriptor |
| 6 | CS | Late collision. Set when collision is active after 64 bytes. This bit is valid only in last descriptor |
| 5 | FT | Frame type. This bit is valid only in last descriptor. 1: Ethernet type 0: 802.3 type |
| 4 | RW | Receive watchdog (refer to CSR15, bit 4). This bit is valid only in last descriptor. |
| 3 | reserved | Default = 0 |
| 2 | DB | Dribble bit. This bit is valid only in last descriptor Packet length is not integer multiple of 8-bit. |
| 1 | CE | CRC error. This bit is valid only in last descriptor |
| 0 | OF | Overflow. This bit is valid only in last descriptor |

RDES1

| Bit # | Name | Descriptions |
|-------|------|--|
| 31~26 | --- | reserved |
| 25 | RER | Receive end of ring indicates this descriptor is last, return to base address of descriptor |
| 24 | RCH | Second address chain Use for chain structure. Indicates the buffer2 address is the next descriptor address. Ring mode takes precedence over chained mode |
| 23~22 | --- | reserved |
| 21~11 | RBS2 | Buffer 2 size (DW boundary) |
| 10~ 0 | RBS1 | Buffer 1 size (DW boundary) |

RDES2

| Bit # | Name | Descriptions |
|-------|------|--|
| 31~0 | RBA1 | Receive Buffer Address 1. This buffer address should be double word aligned. |

RDES3

| Bit # | Name | Descriptions |
|-------|------|--|
| 31~0 | RBA2 | Receive Buffer Address 2. This buffer address should be double word aligned. |

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| | | | |
|-------|-----------------|--------------------|--------------------|
| | 31 | | 0 |
| TDES0 | Own | Status | |
| TDES1 | Control | Buffer2 byte-count | Buffer1 byte-count |
| TDES2 | Buffer1 address | | |
| TDES3 | Buffer2 address | | |

Descriptor addresses must be double word alignment

8.4.2.2. Transmit descriptor description**TDES0**

| Bit # | Name | Descriptions |
|-------|------|--|
| 31 | OWN | Own bit 1: Indicate this descriptor is ready to transmit 0: No transmit data in this descriptor for transmission |
| 30-24 | --- | Reserved |
| 23-22 | UR | Under-run count |
| 21-16 | --- | Reserved |
| 15 | ES | Error summary, OR of the following bit 1: under-run error 8: excessive collision 9: late collision 10: no carrier 11: loss carrier 14: jabber time-out |
| 14 | TO | Transmit jabber time-out |
| 13-12 | ---- | Reserved |
| 11 | LO | Loss carrier |
| 10 | NC | No carrier |
| 9 | LC | Late collision |
| 8 | EC | Excessive collision |
| 7 | HF | Heartbeat fail |
| 6-3 | CC | Collision count |
| 2 | ---- | Reserved |
| 1 | UF | Under-run error |
| 0 | DE | Deferred |

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TDES1

| Bit # | Name | Descriptions |
|-------|------|--|
| 31 | IC | Interrupt completed |
| 30 | LS | Last descriptor |
| 29 | FS | First descriptor |
| 28,27 | --- | Reserved |
| 26 | AC | Disable add CRC function |
| 25 | TER | End of Ring |
| 24 | TCH | 2nd address chain Indicate the buffer2 address is the next descriptor address |
| 23 | DPD | Disable padding function |
| 22 | --- | Reserved |
| 21-11 | TBS2 | Buffer 2 size |
| 10-0 | TBS1 | Buffer 1 size |

TDES2

| Bit # | Name | Descriptions |
|-------|------|--|
| 31~0 | BA1 | Buffer Address 1. Without any limitation on the transmission buffer address. |

TDES3

| Bit # | Name | Descriptions |
|-------|------|--|
| 31~0 | BA2 | Buffer Address 2. Without any limitation on the transmission buffer address. |

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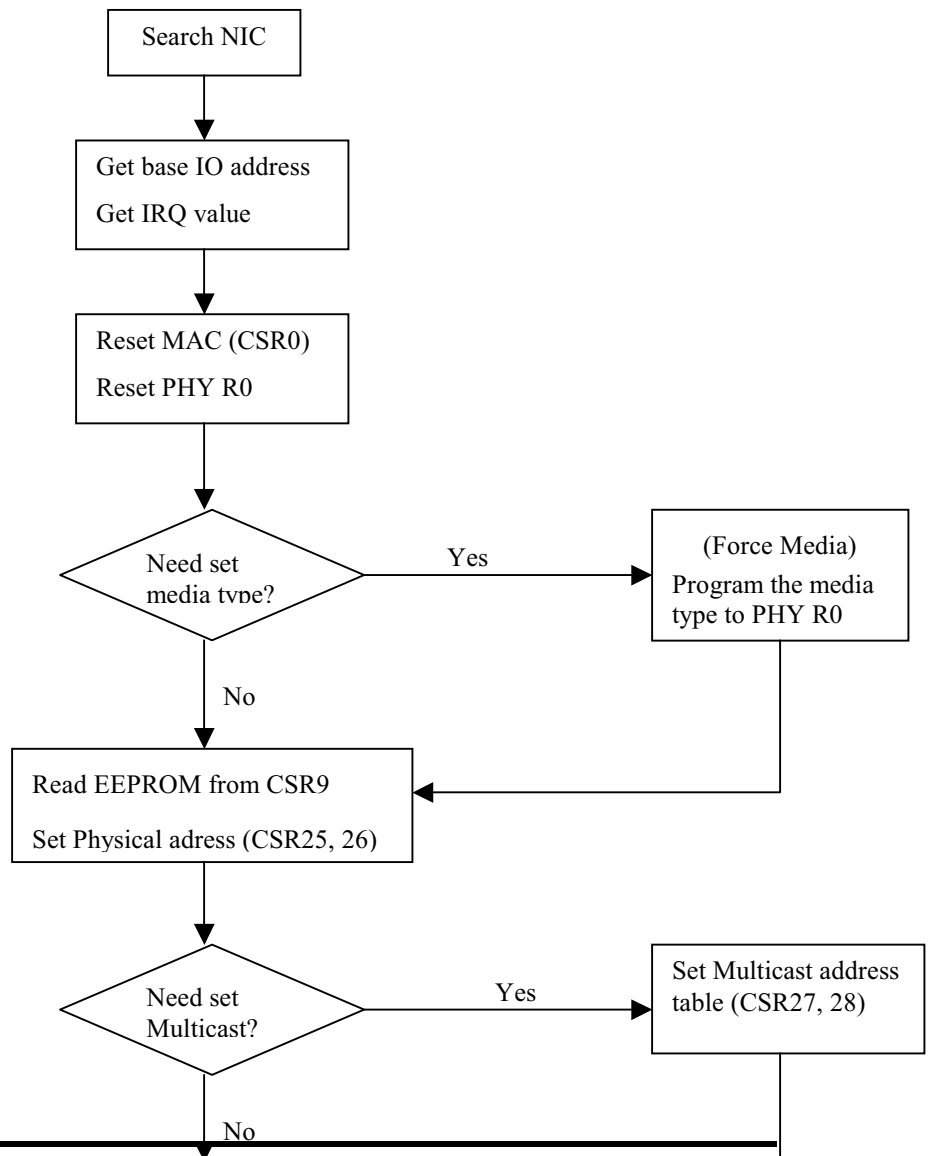
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9. Functional Descriptions

9.1. Initialization Flow

The flow of initialize ADM9511 is shown as below:



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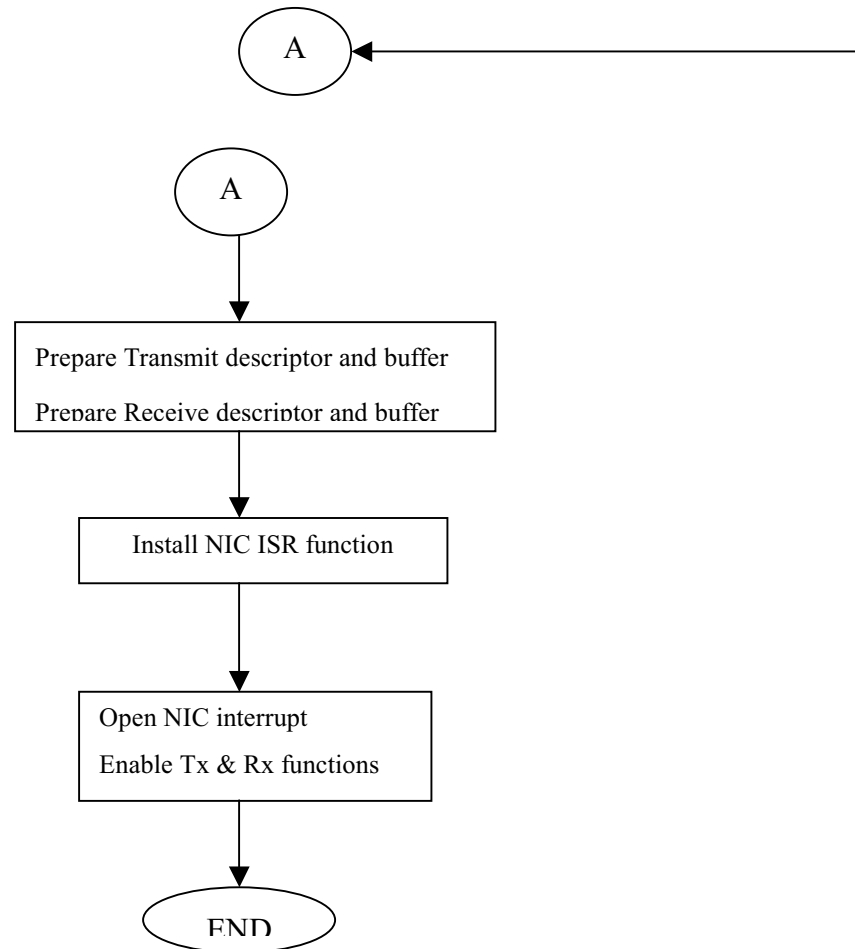
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9.2. Network Packet Buffer Management

9.2.1. Descriptor structure types

For networking operation, the ADM9511 transmits the data packet from transmit buffers in host memory to ADM9511's transmit FIFO and receives the data packet from ADM9511's receive FIFO to receive buffers in host memory. The descriptors that the ADM9511 supports to build in host memory are used as the pointers of these transmit and receive buffers.

There are two structure types for the descriptor, **Ring and Chain**, supported by the ADM9511 and are shown as below. The type selection is controlled by the bit24 of RDES1 and the bit24 of TDES1.

The transmit and receive buffers are physically built in host memory. Any buffer can contain either a whole packet or just part of a packet. But it can't contain more than one packet.

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Ring structure:

There are two buffers per descriptor in the ring structure. Support receive early interrupt.

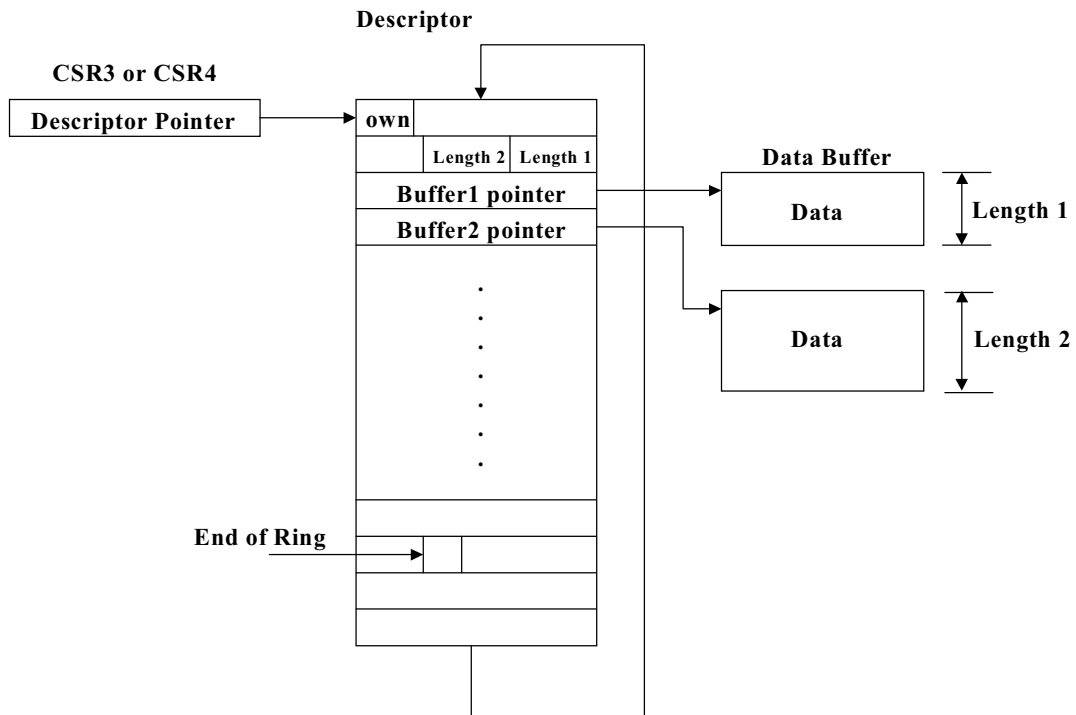


Figure 4 Ring structure of frame buffer

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Chain structure:

There is only one buffer per descriptor in chain structure.

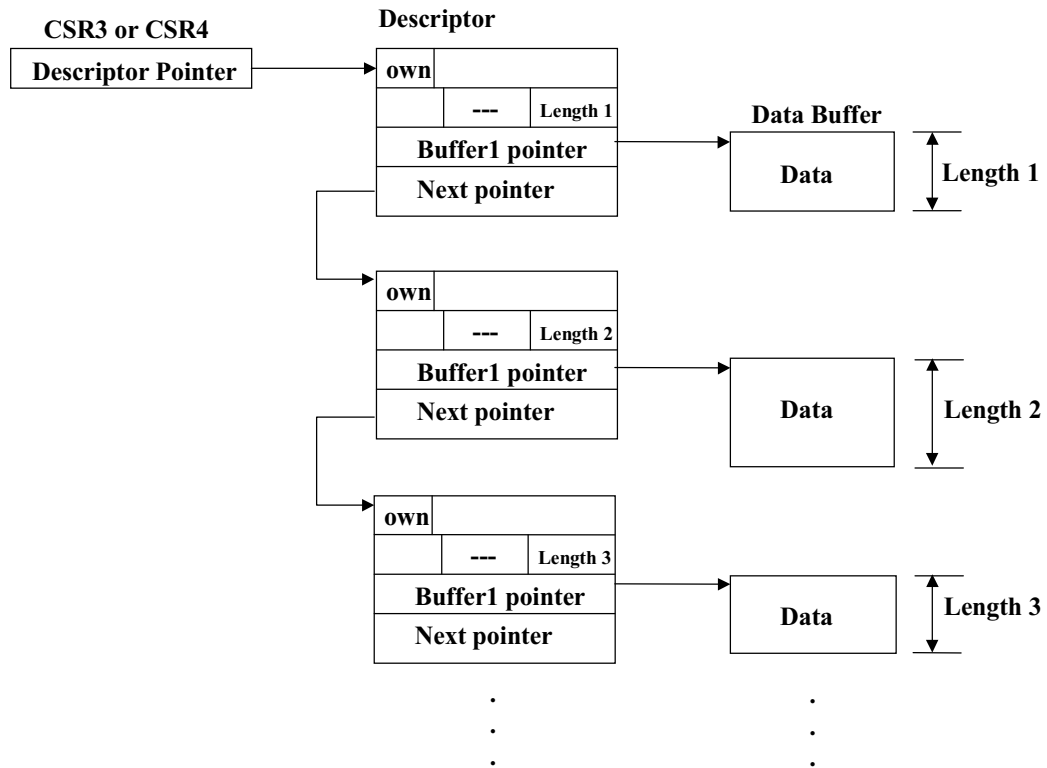


Figure 5 Chain structure of frame buffer

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9.2.2. The point of descriptor management

OWN bit = 1, ready for network side access

OWN bit = 0, ready for host side access

- **Transmit Descriptor Pointers**

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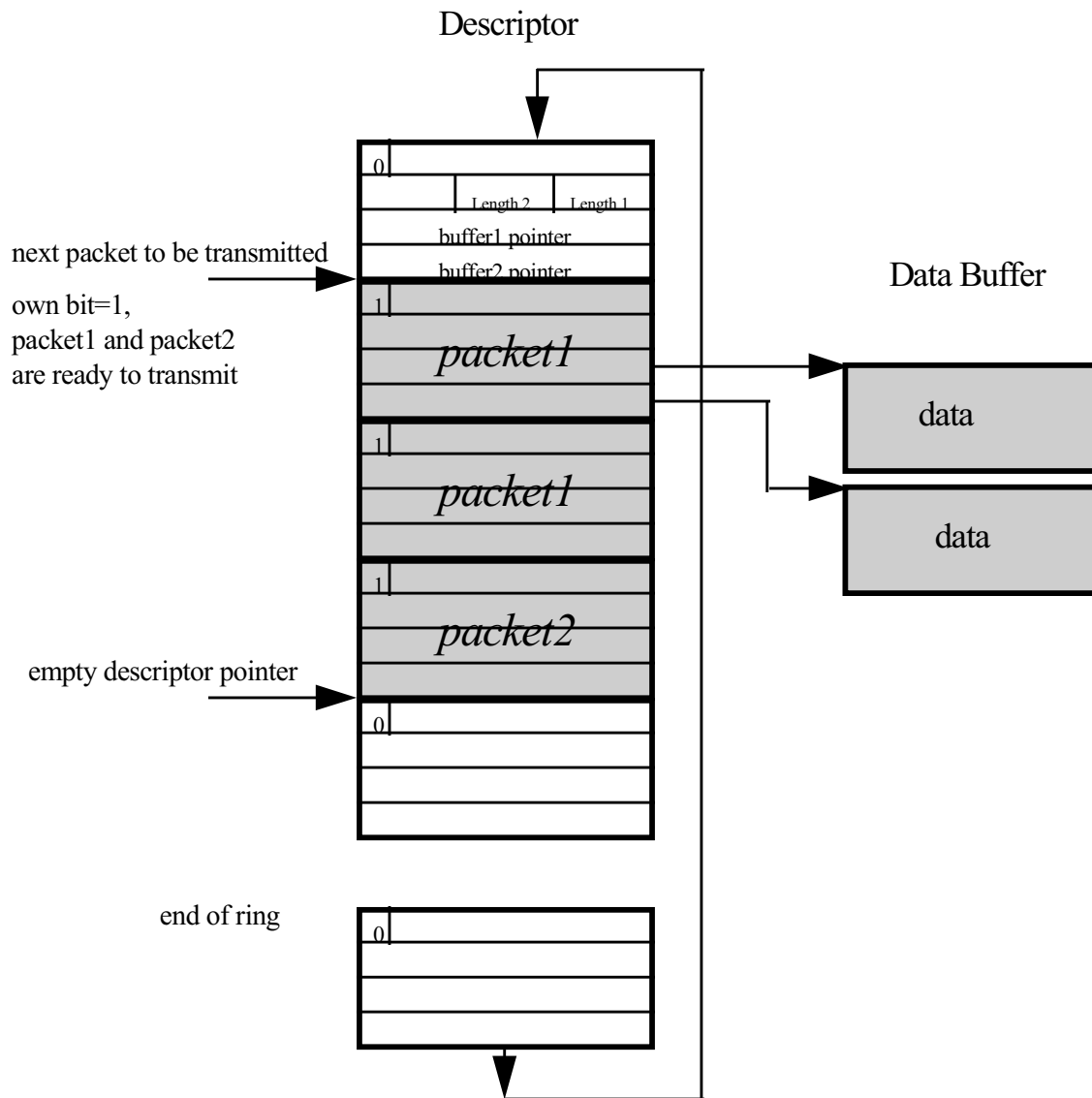
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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****Figure 6 Transmit pointers for descriptor management****ADMtek Inc.**

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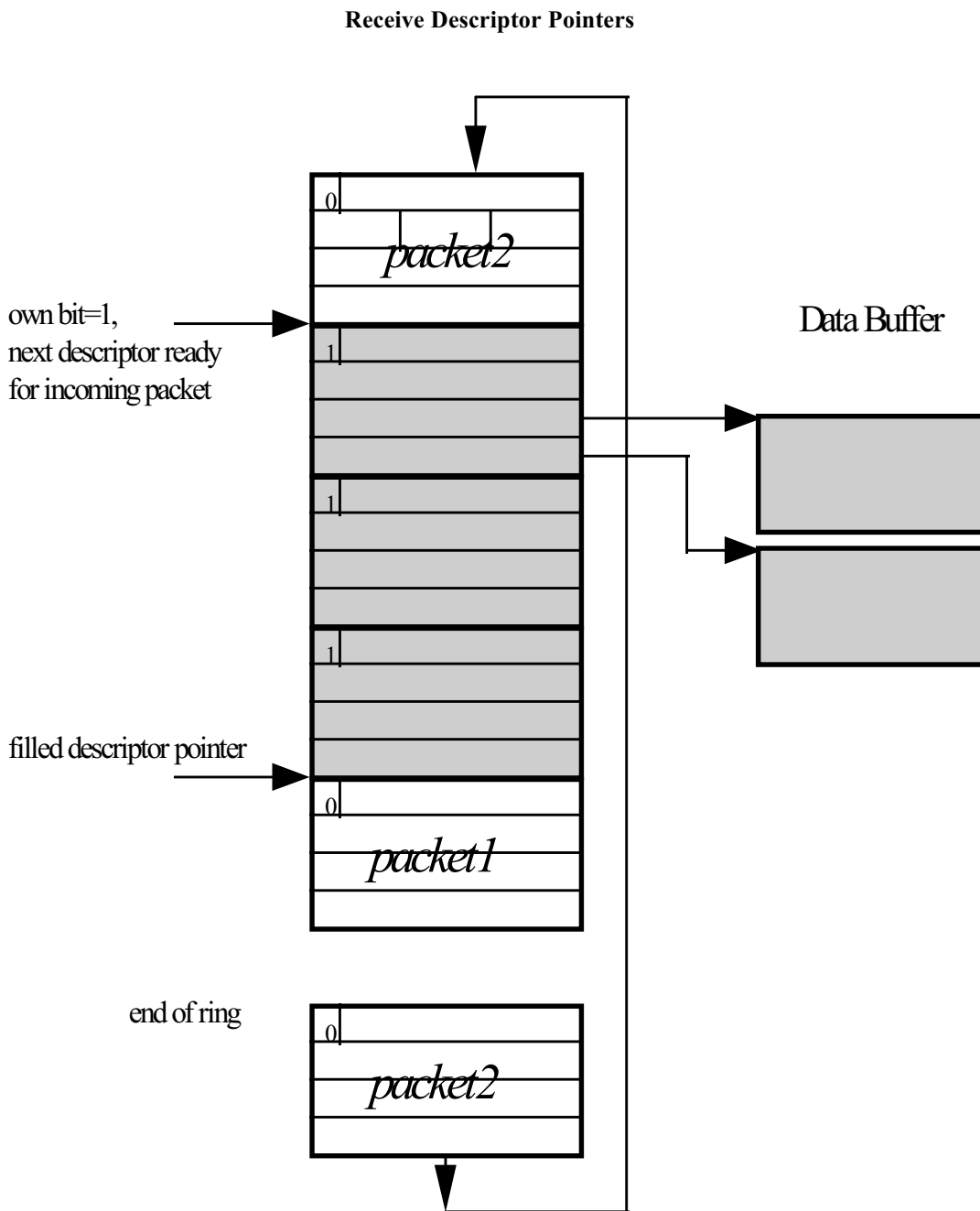
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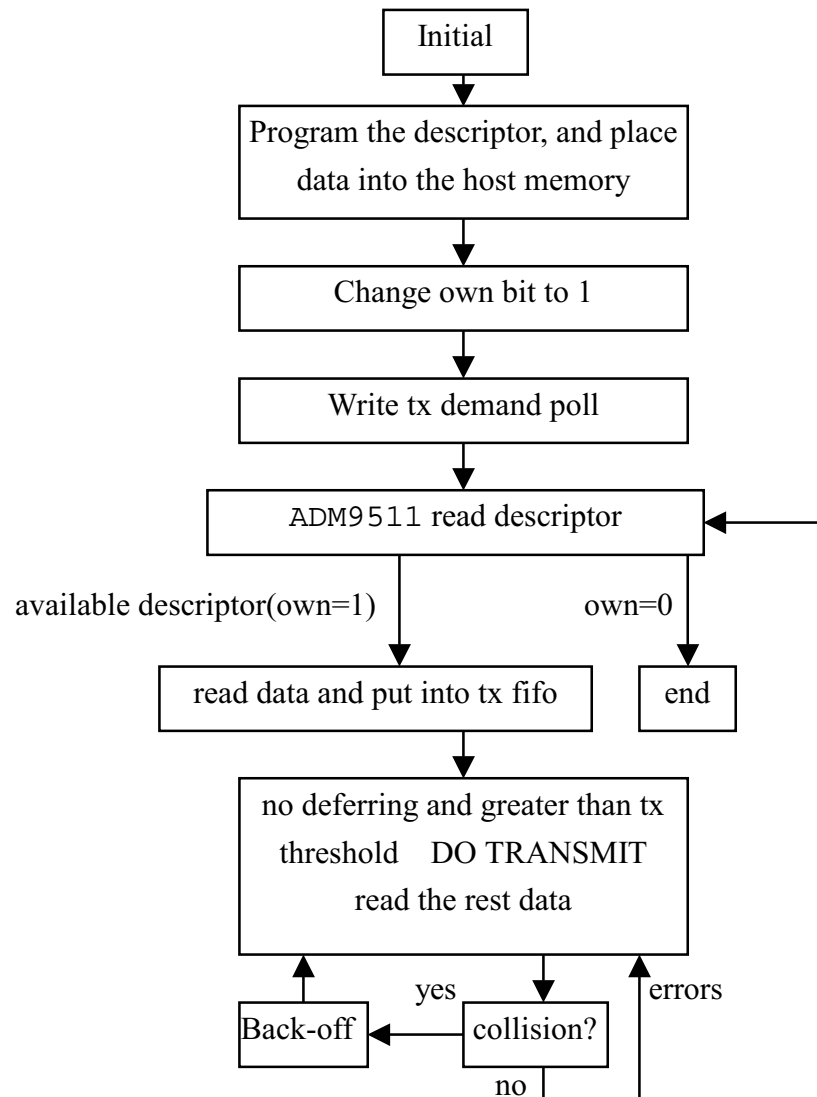
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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****Figure 7 Receive pointers for descriptor management****9.3. Transmit Scheme and Transmit Early Interrupt****9.3.1. Transmit flow**

The flow of packet transmit is shown as below.



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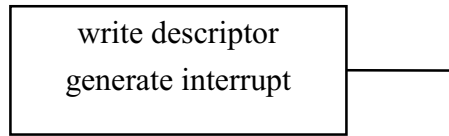
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9.3.2. Transmit pre-fetch data flow

- Transmit FIFO size=2K-byte
- two packets in the FIFO at the same time
- meet the transmit min. back-to-back

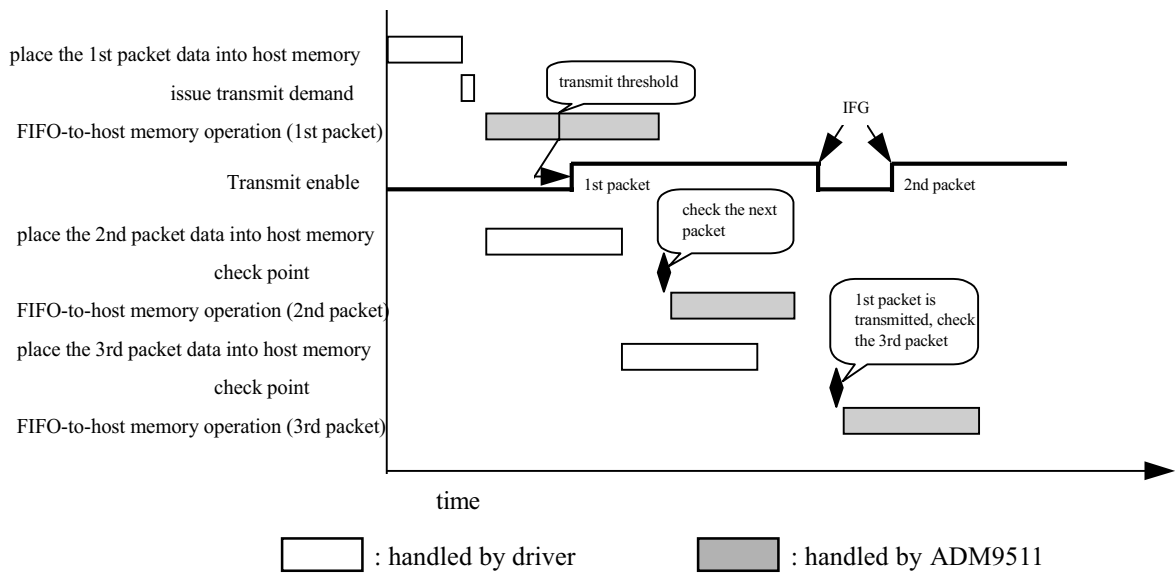


Figure 8 Transmit data flow of pre-fetch data

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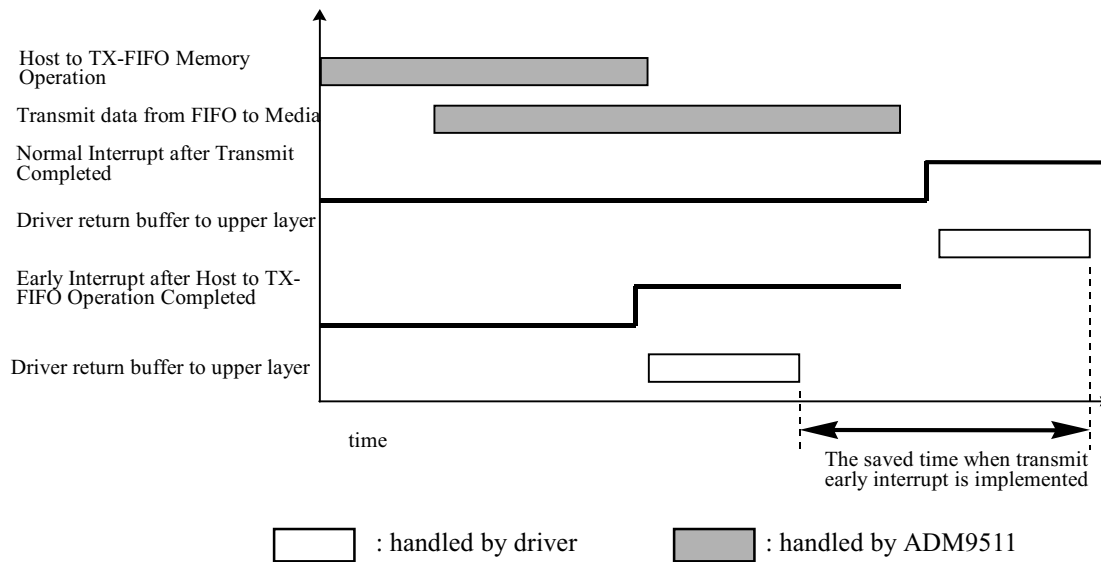
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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****9.3.3. Transmit early interrupt scheme****Figure 9 Transmit normal interrupt and early interrupt comparison**

9.4.Receive Scheme and Receive Early Interrupt Scheme

The following figure shows the difference of timing without early interrupt and with early interrupt.

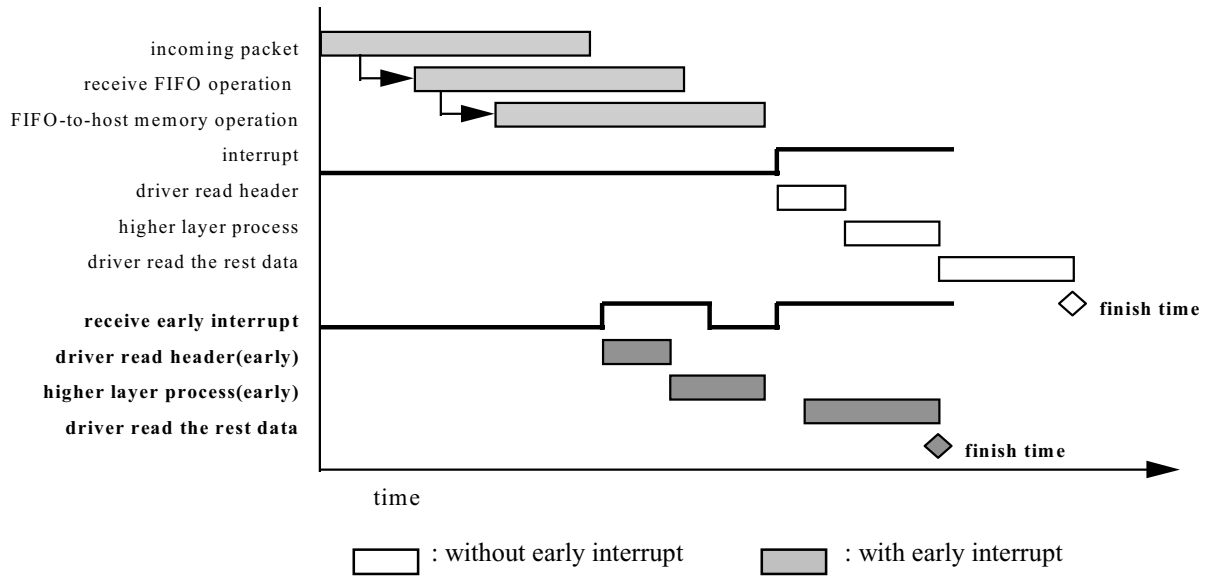
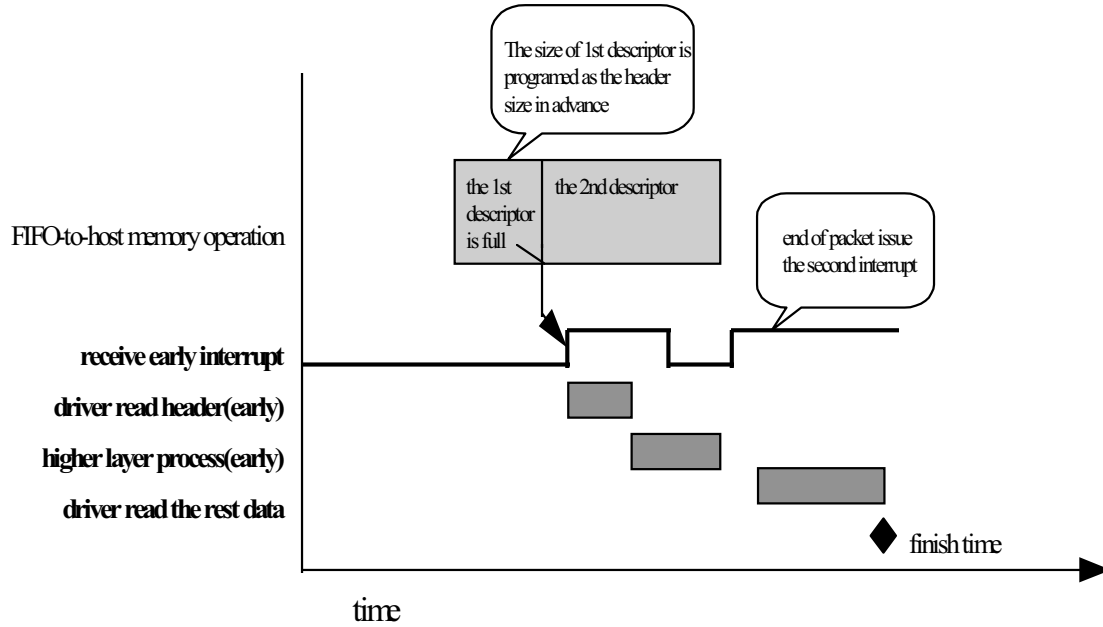


Figure 10 Receive data flow (without early interrupt and with early interrupt)

ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****Figure 11 Detailed Receive Early interrupt flow****ADMtek Inc.**

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9.5. Network Operation

9.5.1. MAC operation

In the MAC (Media Access Control) portion of ADM9511, it incorporates the essential protocol requirements for operating as an IEEE802.3 and Ethernet compliant node.

- **Format**

| Field | Description |
|-----------------------|---|
| Preamble | A 7-byte field of (10101010b) |
| Start Frame Delimiter | A 1-byte field of (10101011b) |
| Destination Address | A 6-byte field |
| Source Address | A 6-byte field |
| Length/Type | A 2-byte field indicated the frame is in IEEE802.3 format or Ethernet format. IEEE802.3 format: 0000H ~ 05DCH for Length field Ethernet format: 05DD ~ FFFFH for Type field |
| Data | *46 ~ 1500 bytes of data information |
| CRC | A 32-bit cyclic redundant code for error detection |

*Note: If padding is disabled(TDES1 bit23), the data field may be shorter than 46 bytes.

- **Transmit Data Encapsulation**

The differences between the encapsulation and a MAC frame while operating in the 100BASE-TX mode are listed as follow:

1. The first byte of the preamble is replaced by the JK code according to the IEEE802.3u, clause 24.
2. After the CRC field of the MAC frame, the ADM9511 inserts the TR code according to the IEEE802.3u, clause 24.

- **Receive Data Decapsulation**

When operate in 100BASE-TX mode the ADM9511 detects a JK code for a preamble as well as a TR code for the packet end. If a JK code is not detected, the ADM9511 will abort this frame receiving and wait for a new JK code detection. If a TR code is not detected, the ADM9511 will report a CRC error.

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- **Deferring**

The Inter-Frame Gap (IFG) time is divided into two parts:

1. IFG1 time (64-bit time): If a carrier is detected on the medium during this time, the ADM9511 will reset the IFG1 time counter and restart to monitor the channel for an idle again.
2. IFG2 time (32-bit time): After counting the IFG2 time the ADM9511 will access the channel even though a carrier has been sensed on the network.

- **Collision Handling**

The scheduling of re-transmissions are determined by a controlled randomization process called “truncated binary exponential back-off”. At the end of enforcing a collision (jamming), the ADM9511 delays before attempting to re-transmit the packet. The delay is an integer multiple of slot time. The number of slot times to delay before the *n*th re-transmission attempt is chosen as a uniform distributed integer *r* in the range:

$$0 \leq r < 2^k \quad \text{where } k = \min(n, 10)$$

9.5.2. Transceiver operation

In the transceiver portion of the ADM9511, it integrates the IEEE802.3u compliant functions of PCS(physical coding sub-layer), PMA(physical medium attachment) sub-layer, and PMD(physical medium dependent) sub-layer for 100BASE-TX, and the IEEE802.3 compliant functions of Manchester encoding/decoding and transceiver for 10BASE-T. All the functions and operation schemes are described in the following sections.

- **100BASE-TX Transmit Operation**

Regarding the 100BASE-TX transmission, the transceiver provides the transmission functions of PCS, PMA, and PMD for encoding of MII data nibbles to five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 Unshielded Twisted Pair cable through an isolation transformer with the turns ratio of 1:1.

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- **Data code-groups Encoder:** In normal MII mode application, the transceiver receives nibble type 4B data via the TXD0~3 inputs of the MII. These inputs are sampled by the transceiver on the rising edge of TX_CLK and passed to the 4B/5B encoder to generate the 5B code-group used by 100BASE-TX.
- **Idle code-groups:** In order to establish and maintain the clock synchronization, the transceiver need to keep transmitting signals to medium. The transceiver will generate Idle code-groups for transmission when there is no real data want to be sent by MAC.
- **Start-of-Stream Delimiter-SSD (/J/K/):** In a transmission stream, the first 16 nibbles are MAC preamble. In order to let partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the transceiver will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.
- **End-of-Stream Delimiter-ESD (/T/R/):** In order to indicate the termination of the normal data transmissions, the transceiver will insert 2 nibbles of /T/R/ code-group after the last nibble of FCS.
- **Scrambling:** All the encoded data(including the idle, SSD, and ESD code-groups) is passed to data scrambler to reduce the EMI and spread the power spectrum using a 10-bit scrambler seed loaded at the beginning.
- **Data conversion of Parallel to Serial, NRZ to NRZI, NRZI to MLT3:** After scrambled, the transmission data with 5B type in 25MHz will be converted to serial bit stream in 125MHz by the parallel to serial function. After serialized, the transmission serial bit stream will be further converted from NRZ to NRZI format. After NRZI converted, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. With this MLT3 code, it lowers the frequency and reduces the energy of the transmission signal in the UTP cable and also makes the system easily to meet the FCC specification of EMI.

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- **Wave-Shaper and Media Signal Driver:** In order to reduce the energy of the harmonic frequency of transmission signals, the transceiver provides the wave-shaper prior the line driver to smooth but keep symmetric the rising/falling edge of transmission signals. The wave-shaped signals include the 100BASE-TX and 10BASE-T both are passed to the same media signal driver. This design can simplify the external magnetic connection with single one.

- **100BASE-TX Receiving Operation**

Regarding the 100BASE-TX receiving operation, the transceiver provides the receiving functions of PMD, PMA, and PCS for receiving incoming data signals through category 5 UTP cable and an isolation transformer with turns ratio of 1: 1. It includes the adaptive equalizer and baseline wander, data conversions of MLT3 to NRZI, NRZI to NRZ and serial to parallel, the PLL for clock and data recovery, the de-scrambler, and the decoder of 5B/4B.

- **Adaptive Equalizer and Baseline Wander:** Since the high speed signals over the unshielded (or shielded) twisted Pair cable will induce the amplitude attenuation and phase shifting. Furthermore, these effects are depends on the signal frequency, cable type, cable length and the connectors of the cabling. So a reliable adaptive equalizer and baseline wander to compensate all the amplitude attenuation and phase shifting are necessary. In the transceiver, it provides the robust circuits to perform these functions.
- **MLT3 to NRZI Decoder and PLL for Data Recovery:** After receiving the proper MLT3 signals, the transceiver converts the MLT3 to NRZI code for further processing. After adaptive equalizer, baseline wander, and MLT3 to NRZI decoder, the compensated signals with NRZI type in 125MHz are passed to the Phase Lock Loop circuits to extract out the original data and the synchronous clock.
- **Data Conversions of NRZI to NRZ and Serial to Parallel:** After data recovered, the signals will be passed to the NRZI to NRZ converter to generate the 125MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing.

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- **De-scrambling and Decoding of 5B/4B:** The parallel 5B type data is passed to de-scrambler and 5B/4B decoder to return their original MII nibble type data.
- **Carrier sensing:** Carrier Sense(CRS) signal is asserted when the transceiver detects any 2 non-contiguous zeros within any 10bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or receive. But in full duplex mode, CRS is asserted only during packet reception.

- **10BASE-T Transmission Operation**

It includes the parallel to serial converter, Manchester Encoder, Link test function, Jabber function and the transmit wave-shaper and line driver described in the section of “Wave-Shaper and Media Signal Driver” of “100BASE-T Transmission Operation”. It also provides Collision detection and SQE test for half duplex application.

- **10BASE-T Receive Operation**

It includes the carrier sense function, receiving filter, PLL for clock and data recovering, Manchester decoder, and serial to parallel converter.

- **Loop-back Operation of transceiver**

The transceiver provides internal loop-back (also called transceiver loop-back) operation for both the 100BASE-TX and 10BASE-T operations. The loop-back operation can be enabled by setting bit 14 of PHY register 0 to 1. In this loop-back operation, the TX± and RX± lines are isolated from the media. The transceiver also provides remote loop-back operation for 100BASE-TX operation. The remote loop-back operation can be enabled by setting bit 3 of PHY register 21 to 1.

In the 100BASE-TX internal loop-back operation, the data comes from the transmit output of NRZ to NRZI converter then loop-back to the receive path into the input of NRZI to NRZ converter.

In the 100BASE-TX remote loop-back operation, the data is received from RX± pins through receive path to the output of data and clock recover and then loop-back to the input of NRZI to MLT3

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converter of transmit path then transmit out to the medium via the transmit line drivers.

In the 10BASE-T loop-back operation, the data is through transmit path and loop-back from the output of the Manchester encoder into the input of Phase Lock Loop circuit of receive path.

- **Full Duplex and Half Duplex Operation of Transceiver**

The transceiver can operate for either full duplex or half duplex network application. In full duplex, both transmit and receive can be operated simultaneously. Under full duplex mode, collision(COL) signal is ignored and carrier sense(CRS) signal is asserted only when the transceiver is receiving.

In half duplex mode, either transmit or receive can be operated at one time. Under half duplex mode, collision signal is asserted when transmit and receive signals collided and carrier sense asserted during transmission and reception.

- **Auto-Negotiation Operation**

The Auto-Negotiation function is designed to provide the means to exchange information between the transceiver and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation function can be controlled through bit 12 of PHY register 0.

The Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses(FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partner's capabilities which are determined by PHY register 4. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100BASE-TX full duplex
2. 100BASE-TX half duplex
3. 10BASE-T full duplex
4. 10BASE-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled then FLPs will be transmitted and the Auto-Negotiation function will process. Otherwise, the Auto-Negotiation will not occur until the bit 12 of PHY register 0 is set to 1. When the Auto-Negotiation is disabled, then the Network Speed and Duplex Mode are selected by programming PHY register 0.

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- **Power Down Operation**

To reduce the power consumption the transceiver is designed with power down feature which can save the power consumption significantly. Since the power supply of the 100BASE-TX and 10BASE-T circuits are separated, the transceiver can turn off the circuit of either the 100BASE-TX or 10BASE-T when the other one of them is operating.

9.5.3. Flow control in full duplex application

The PAUSE function operation is used to inhibit transmission of data frames for a specified period of time. The ADM9511 supports full duplex protocol of IEEE802.3x. To support PAUSE function, the ADM9511 implements the MAC Control Sub-layer functions to decode the MAC Control frames received from MAC control clients and execute the relative requests accordingly. When the Full Duplex mode and PAUSE function are selected after Auto-Negotiation completed, then the ADM9511 enables the PAUSE function for flow control of full duplex application. In this section we will describe how the ADM9511 implements the PAUSE function.

- **MAC Control Frame and PAUSE Frame**

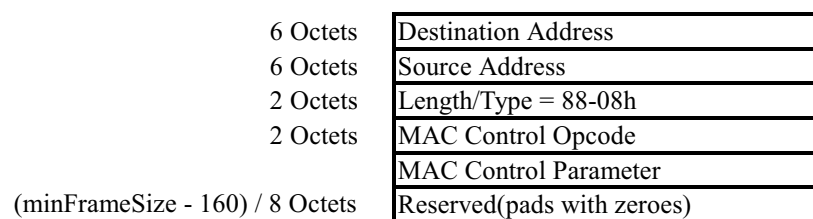


Figure 12 MAC Control Frame Format

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The MAC control frame is distinguished from other MAC frames only by their Length/Type field identifier. The MAC Control Opcode defined in MAC Control Frame format for PAUSE function is 0001h. Besides, the PAUSE time is specified in the MAC Control Parameters field with 2 Octets, unsigned integer, in the units of Slot-Times. The range of possible PAUSE time is 0 to 65535 Slot-Times.

So, a valid PAUSE frame issued by a MAC control client(could be a switch or a bridge) will contain:

- The destination address is set equal to the globally assigned 48 bit multicast address 01-80-C2-00-00-01, or equal to the unicast address which the MAC control client wishes to inhibit its transmission of data frames.
- Filled the MAC Control Opcode field with 0001h.
- 2 Octets of PAUSE time specified in the MAC Control parameter field to indicate the length of time for which the destination is wished to inhibit data frame transmission.

● **Receive Operation for PAUSE function**

Upon reception of a valid MAC Control frame, the ADM9511 will start a timer for the length of time specified by the MAC Control Parameters field. When the timer value reaches zero then the ADM9511 ends PAUSE state. However, a PAUSE frame should not affect the transmission of a frame that has been submitted to the MAC(started Transmit out of the MAC and can't be interrupted). On the other hand, the ADM9511 shall not begin to transmit a frame more than one Slot-Times after received a valid PAUSE frame with a non-zero PAUSE time. If the ADM9511 receives a PAUSE frame with a zero PAUSE time value, then the ADM9511 ends the PAUSE state immediately.

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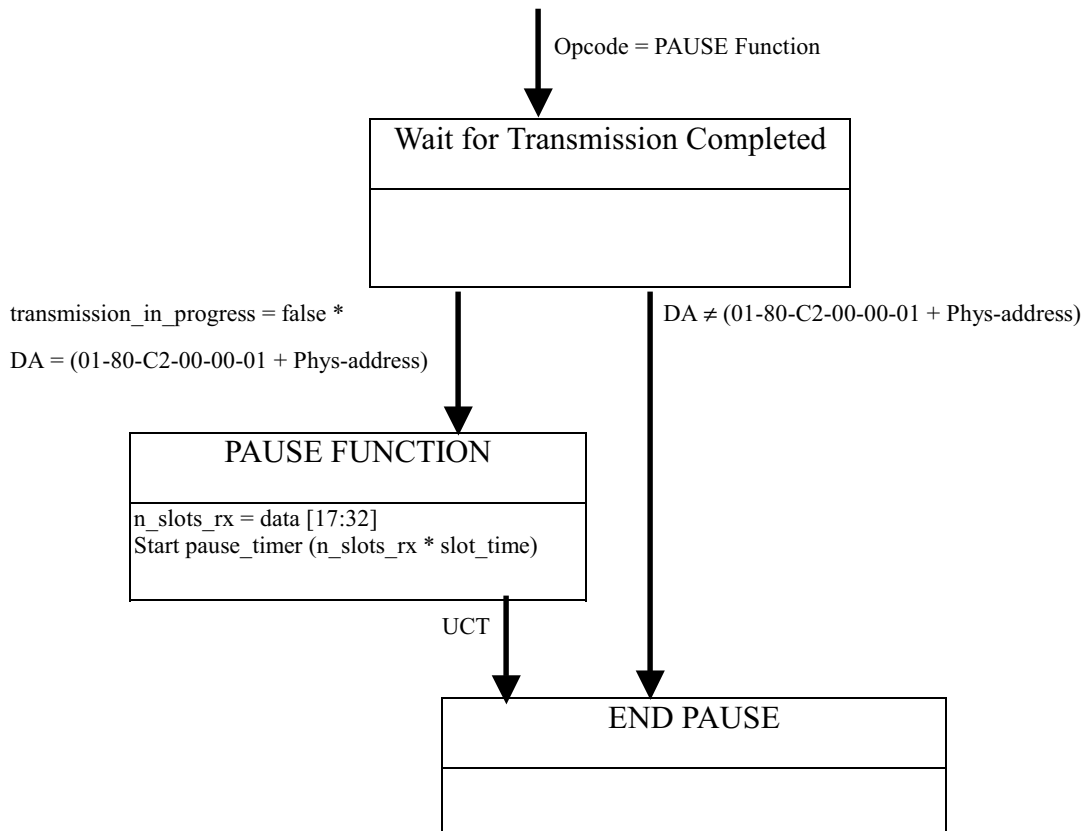


Figure 13 PAUSE operation receive state diagram

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9.6.Reset Operation

9.6.1. Reset whole chip

There are two ways to reset the ADM9511. First, hardware reset, the ADM9511 can be reset via RST# pin. For ensuring proper reset operation, at least 100 μ s active Reset input signal is required. Second, software reset, when bit 0 of CSR0 register is set to 1, the ADM9511 will reset entire circuits and register to default value then clear the bit 0 of CSR0 to 0.

9.6.2. Reset Transceiver only

When bit 15 of PHY register 0 is set to 1, the transceiver will reset entire circuits and register contains to default value then clear the bit 15 of PHY register 0 to 0.

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9.7.Wake-on-LAN function

The ADM9511 can assert a signal to wake up the system when it received a Magic Packet from the network. The Wake on LAN operation is described as follow.

- **The Magic Packet format:**

- Valid destination address that can pass the address filter of the ADM9511
- The payload of frame must include at least 6 contiguous 'FF' followed immediately by 16 repetitions of IEEE address.
- The frame can contain multiple 'six FF + sixteen IEEE address' pattern.
- CRC OK

- **The Wake on LAN operation**

The Wake on LAN enable function is controlled by bit 18 of CSR18, it is loaded from EEPROM after reset or programmed by driver to enable Wake on LAN function. If the bit 18 of CSR18 is set and the ADM9511 receive a Magic Packet, it will assert the PME# signal (drive to low) to indicate receiving a wake up frame as well as to set the PME status bit (the bit 15 of CSR20).

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9.8.ACPI Power Management function

The ADM9511 has a built-in capability for Power Management (PM) which controlled by the host system

The ADM9511 will provide:

- Compatibility with Device Class Power Management Reference Specification, Rev1.09
- Compatibility with ACPI specification, Rev 1.0
- Compatibility with PCI Bus Power Management Interface Specification, Rev 1.1
- Compatibility with AMD Magic Packet™ Technology.
- Compatibility with PCI CLKRUN scheme.

9.8.1. Power states

- **D0 (Fully On)**

In this state the ADM9511 operates as full functionality and consumes its normal power. While in the D0 state, if the PCI clock is lower than 16MHz, the ADM9511 may not receive or transmit frames properly.

- **D1**

In this state the ADM9511 doesn't response to any accesses except configuration space and full function context in place. The only network operation the ADM9511 can initiate is a wake-up event.

- **D2**

In this state the ADM9511 only respond to access configuration space and full function context in place. The ADM9511 can't transmit or receive even the wake-up frame.

- **D3_{cold} (Power Removed)**

In this state all function context is lost. When power is restored, the function will return to D0.

- **D3_{hot} (Software Visible D3)**

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When the ADM9511 is brought back to D0 from D3_{hot} the software must perform a full initialization.

The ADM9511 in the D3_{hot} state respond to configurations cycles as long as power and clock are supplied. This requires the device to perform an internal reset and return to a power-up reset condition without the RST# pin asserted.

| Device State | PCI Bus State | Function Context | Clock | Power | Supported Actions to Function | Supported Actions from Function |
|--------------|---------------|--|-----------------------|------------|----------------------------------|----------------------------------|
| D0 | B0 | Full function context in place | Full speed | Full power | Any PCI transaction | Any PCI transaction or interrupt |
| D1 | B0, B1 | Configuration maintained. No Tx and Rx except wake-up events | Stopped to Full speed | | PCI configuration access | Only wake-up events |
| D2 | B0, B1, B2 | Configuration maintained. No Tx and Rx | Stopped to Full speed | | PCI configuration access(B0, B1) | |
| D3hot | B0, B1, B2 | Configuration lost, full initialization required upon return to D0 | Stopped to Full speed | | PCI configuration access(B0, B1) | |
| D3cold | B3 | All configuration lost. Power-on defaults in place on return to D0 | No clock | No power | Power-on reset | |

Table 1 Power state

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9.9. Modem Operation

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9.10. LED Display Operation

The ADM9511 provides 2 kinds of LED display mode for Ethernet networking, the detail descriptions about the operation are described in the PIN Description section.

- First mode - 3 LED displays for
 - ◆ 100Mbps(on) or 10Mbps(off)
 - ◆ Link(Keeps on when link ok) or Activity(Blink with 10Hz when receiving or transmitting but not collision)
 - ◆ FD(Keeps on when in Full duplex mode) or Collision(Blink with 20Hz when colliding)
- Second mode – 4 LED displays for
 - ◆ 100 Link(On when 100M link ok)
 - ◆ 10 Link(On when 10M link ok)
 - ◆ Activity (Blink with 10Hz when receiving or transmitting)
 - ◆ FD(Keeps on when in Full duplex mode) or Collision(Blink with 20Hz when colliding)

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****10. General EEPROM Format Description**

| Offset | Length | Description |
|--------|--------|--|
| 0 | 2 | ADM9511 <i>Signature</i> : 0x9511 |
| 2 | 1 | Format major version: 0x01 . |
| 3 | 1 | Format minor version: 0x00 |
| 4 | 4 | Reserved |
| 8 | 6 | IEEE network address: ID1, ID2, ID3, ID4, ID5, ID6 (auto load to CSR25/26) |
| E | 2 | Reserved, should be zero . |
| 10 | 2 | Reserved, should be zero . |
| 12 | 2 | <i>Default Connection Type</i> , See Table 3 |
| 14 | 1 | BootRom ENABLE=1 , DISABLE=0 (auto load to CR12, BRE bit) |
| 15 | 1 | BootRom Default selection: 0: Using INT 18h 1: Using INT 19h 2: Using PnP/BEV (BBS) 0x10: Boot From RPL |
| 16 | 10 | Reserved, should be zero . |
| 20 | 2 | PCI <i>Device ID</i> : 0x9511 (auto load to CR0, LDID bits) |
| 22 | 2 | PCI <i>Vendor ID</i> : 0x1317 (auto load to CR0, LVID bits) |
| 24 | 2 | PCI <i>Subsystem ID</i> (auto load to CR11, SID bits) |
| 26 | 2 | PCI <i>Subsystem Vendor ID</i> (auto load to CR11 SVID bits) |
| 28 | 1 | MIN_GNT value. 0xFF (auto load to CR15 & MCR15, MG bits) |
| 29 | 1 | MAX_LAT value. 0xFF (auto load to CR15 & MCR15, ML bits) |
| 2A | 4 | LAN CIS Pointer, 0x0202 (auto load to CR10) |
| 2E | 2 | CSR18 (CR) bit 31-16 recall data. Please refer to CSR18 bit definition |
| 30 | 2 | Modem Device ID: 0x9512 (auto load to MCR0, LDID bits) |
| 32 | 2 | Modem Vendor ID: 0x1317 (auto load to MCR0, LVID bits) |
| 34 | 2 | Modem Subsystem ID (auto load to MCR11, SID bits) |
| 36 | 2 | Modem Subsystem Vendor ID (auto load to MCR11, SVID bits) |
| 38 | 1 | Modem SubClass ID, 0x03 (auto load to MCR2 SC bits) |
| 39 | 1 | Reserved |
| 3A | 1 | Modem Revision Number, 0x02 (auto load to MCR2, RN&SN bits) |
| 3B | 1 | Reserved |
| 3C | 4 | Modem CIS Pointer, 0x0102 (auto load to MCR10) |
| 40 | 1 | Ethernet power consumption on D1, D2, D3 states (auto load to CR49 Data Register) |
| 41 | 1 | Ethernet power consumption on D0 states (auto load to CR49 Data Register) |
| 42 | 1 | Modem power consumption on D1, D2, D3 states (auto load to MCR49 Data Register) |

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| | | |
|-----|-----|---|
| 43 | 1 | Modem power consumption on D0 state (auto load to MCR49 Data Register) |
| 44 | 1 | CSR29 recall data, please refer to the CSR29 bit definition |
| 46 | 10 | Reserved, should be zero |
| 50 | 2 | Modem CIS word count (< 128 bytes) (auto load to CSR15a MCIScnt bits) |
| 52 | 2 | LAN CIS word count (< 128 bytes) (auto load CSR15a CIScnt bits) |
| 54 | 42 | Reserved, should be zero . |
| 7E | 2 | <i>Checksum</i> , the least significant two bytes of FCS for data stored in offset 0..7D of EEPROM |
| 80 | 192 | Modem CIS DATA |
| 140 | 192 | LAN CIS DATA |

Table 3 Connection Type Definition

| | |
|--------|-------------------------|
| 0xFFFF | Software Driver Default |
| 0x0100 | Auto-Negotiation |
| 0x0200 | Power-on Auto-detection |
| 0x0400 | Auto Sense |
| 0x0000 | 10BaseT |
| 0x0001 | BNC |
| 0x0002 | AUI |
| 0x0003 | 100BaseTx |
| 0x0004 | 100BaseT4 |
| 0x0005 | 100BaseFx |
| 0x0010 | 10BaseT Full Duplex |
| 0x0013 | 100BaseTx Full Duplex |
| 0x0015 | 100BaseFx Full Duplex |

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11. Electroical Specifications and Timings

11.1 Absolute Maximum Ratings

| | |
|---------------------|--------------------|
| Supply Voltage(Vcc) | -0.5V to 3.6V |
| Input Voltage | -0.5V to VCC+0.5 V |
| Output Voltage | -0.5V to VCC+0.5 V |
| Storage Temperature | -65°C to 150°C |
| Ambient Temperature | 0°C to 70°C |
| ESD Protection | 2000V |

DC Specifications

General DC Specifications

| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|----------------|-----------|-----|---------|-----|-------|
| Vcc | Supply Voltage | | 3.0 | | 3.6 | V |
| Icc | Power Supply | | | | 1 | A |

PCI Interface DC Specifications

| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|-----------------------|-------------|----------|---------|----------|-------|
| Vilp | Input LOW Voltage | | -0.5 | | 0.325vcc | V |
| Vihp | Input HIGH Voltage | | 0.475vcc | | Vcc+0.5 | V |
| Iilp | Input Leakage Current | 0<Vin <Vcc | | | +10 | uA |
| Volp | Output LOW Voltage | Iout=700uA | | | 0.1Vcc | V |
| Vohp | Output HIGH Voltage | Iout=-150uA | 0.9Vcc | | | V |
| Cinp | Input Pin Capacitance | | 5 | | 17 | pF |
| Cclkp | CLK Pin Capacitance | | 10 | | 22 | pF |

Flash/EEPROM Interface DC Specifications

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| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|-----------------------|-----------|-----------------------|---------|-----------------------|-------|
| Vilf | Input LOW Voltage | | 0 | | V _{cc} x 0.3 | V |
| Vihf | Input HIGH Voltage | | V _{cc} x 0.7 | | V _{cc} + 1 | V |
| Iif | Input Leakage Current | | | | ? | uA |
| Volf | Output LOW Voltage | | | | 0.2 | V |
| Vohf | Output HIGH Voltage | | V _{cc} - 0.2 | | | V |
| Cinf | Input Pin Capacitance | | | | ? | pF |

11.2 AC Specifications**PCI Signaling AC Specifications for 3.3V**

| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|---------------------------|---------------|------|---------|-----|-------|
| Ioh(AC) | Switching Current High | | | 4 | | mA |
| Iol(AC) | Switching Current Low | | | 6 | | mA |
| | Slew Rate | | 0.25 | | 1 | V/ns |
| Icl | Low Clamp Current | | | | | mA |
| Tr | Unloaded Output Rise Time | 0.2vcc~0.6vcc | 1 | | 4 | V/ns |
| Tf | Unloaded Output Fall Time | 0.6vcc~0.2vcc | 1 | | 4 | V/ns |

11.3 Timing Specifications**PCI Clock Specifications**

| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|------------------|-----------|-----|---------|-----|-------|
| Tcyc | Clock Cycle Time | | 30 | | | ns |
| Thigh | Clock High Time | | 12 | | | ns |
| Tlow | Clock Low Time | | 12 | | | ns |

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| | | | | |
|-----------------|--|---|---|------|
| Clock Slew Rate | | 1 | 4 | V/ns |
|-----------------|--|---|---|------|

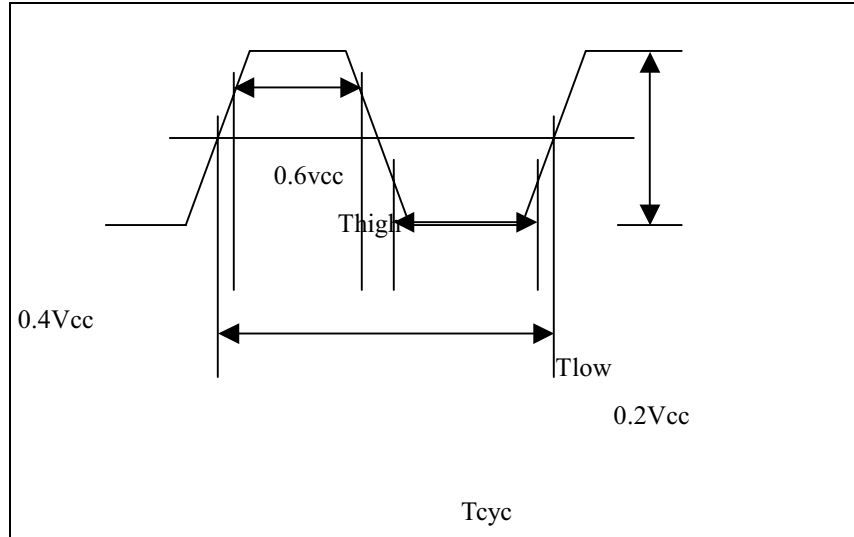


Figure 13 PCI Clock Waveform

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****PCI Timings**

| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|---|-----------|-------|---------|-----|-------|
| Tval | access time – bused signals | | 2 | | 11 | ns |
| Tval(ptp) | access time –point to point | | 2 | | 12 | ns |
| Ton | Float to Active Delay | | 2 | | | ns |
| Toff | Active to Float Delay | | | | 28 | ns |
| Tsu | Input Set up Time to Clock – bused signals | | 7 | | | ns |
| Tsu(ptp) | Input Set up Time to Clock - point to point | | 10,12 | | | ns |
| Th | Input Hold Time from Clock | | 0 | | | ns |
| Trst | Reset Active Time after Power Stable | | 1 | | | ms |
| Trst-clk | Reset Active Time after CLK Stable | | 100 | | | us |
| Trst-off | Reset Active to Output Float delay | | | | 40 | ns |

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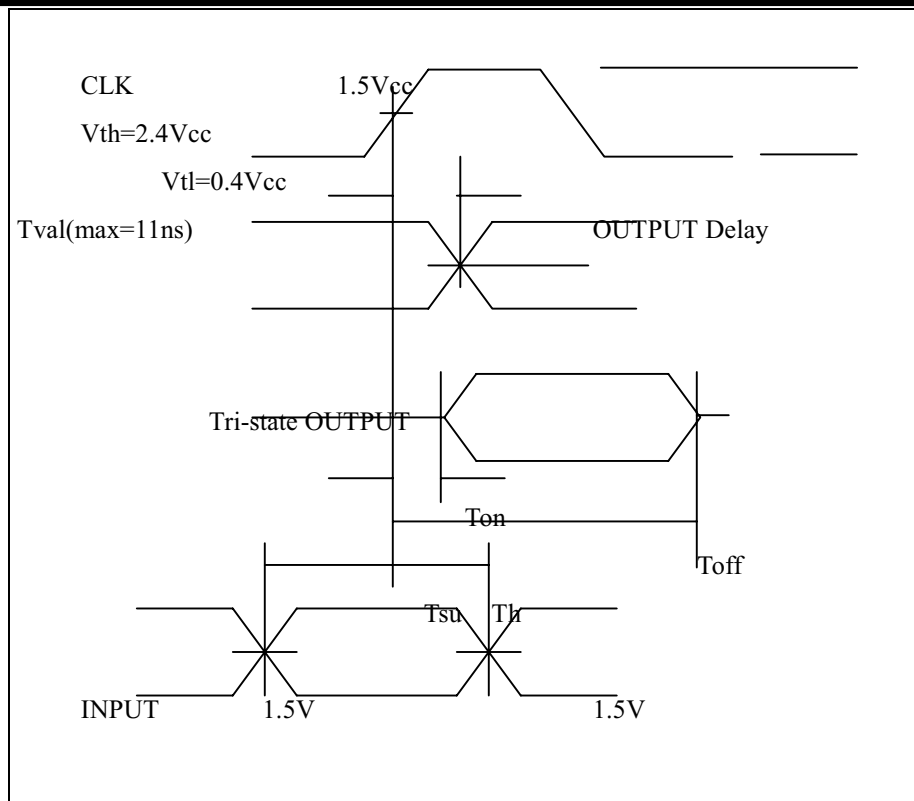


Figure 14 PCI Timings

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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****Flash Interface Timings**

| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|---------------------------------|-----------|------|---------|-----|-------|
| Trc | Read cycle time | | 90 | | | ns |
| Tce | Chip enable access time | | | | 90 | ns |
| Taa | Address access time | | | | 90 | ns |
| Toe | Output enable access time | | | | 45 | ns |
| Tclz | #CE low to active output | | 0 | | | ns |
| Tolz | #OE low to active output | | 0 | | | ns |
| Tchz | #CE high to active output | | | | 45 | ns |
| Tohz | #OE high to active output | | | | 45 | ns |
| Toh | Output hold from address change | | 0 | | | ns |
| Twc | Write cycle time | | | | 10 | ms |
| Tas | Address setup time | | 0 | | | ns |
| Tah | Address hold time | | 50 | | | ns |
| Tcs | #WE and #CE setup time | | 0 | | | ns |
| Tch | #WE and #CE hold time | | 0 | | | ns |
| Toes | #OE high setup time | | 10 | | | ns |
| Toeh | #OE high hold time | | 10 | | | ns |
| Tcp | #CE pulse width | | 70 | | | ns |
| Twp | #WE pulse width | | 70 | | | ns |
| Twph | #WE high width | | 150 | | | ns |
| Tds | Data setup time | | 50 | | | ns |
| Tdh | Data hold time | | 10 | | | ns |
| Tblc | Byte load cycle time | | 0.22 | | 200 | us |
| Tblco | Byte load cycle time out | | 300 | | | us |

Figure 15 Flash write timings**ADMtek Inc.**

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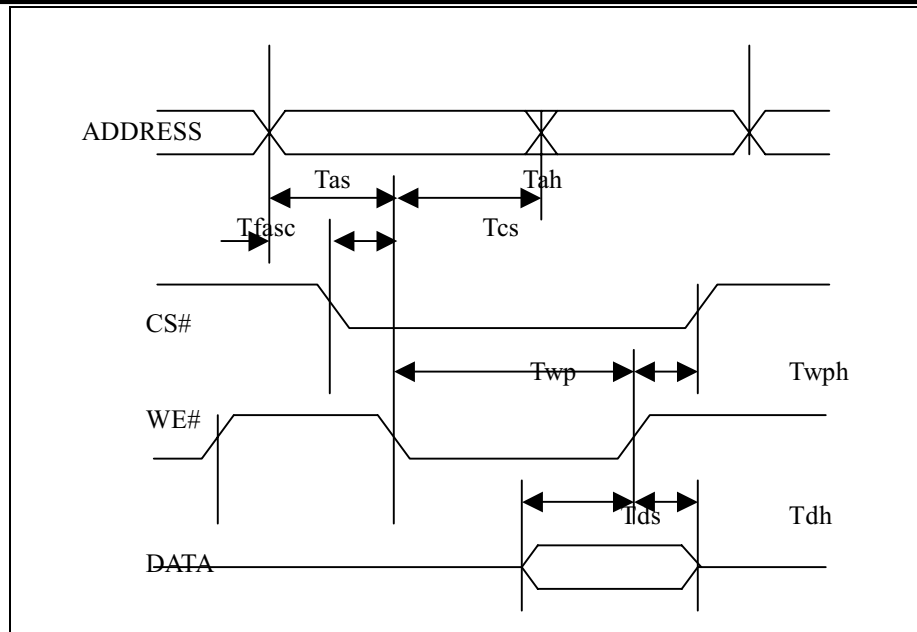
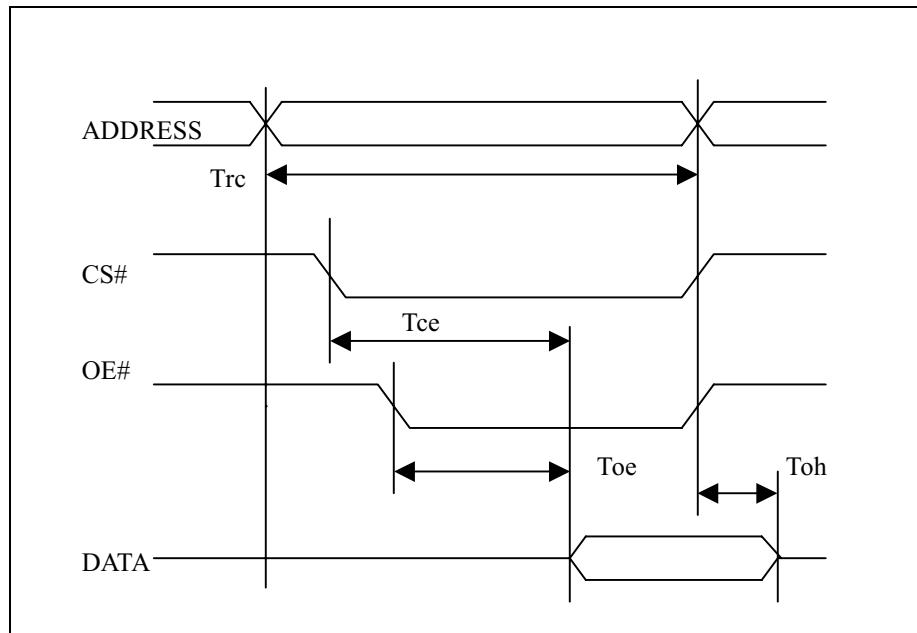


Figure 16 Flash read timings



EEPROM Interface Timings (AC/AD)

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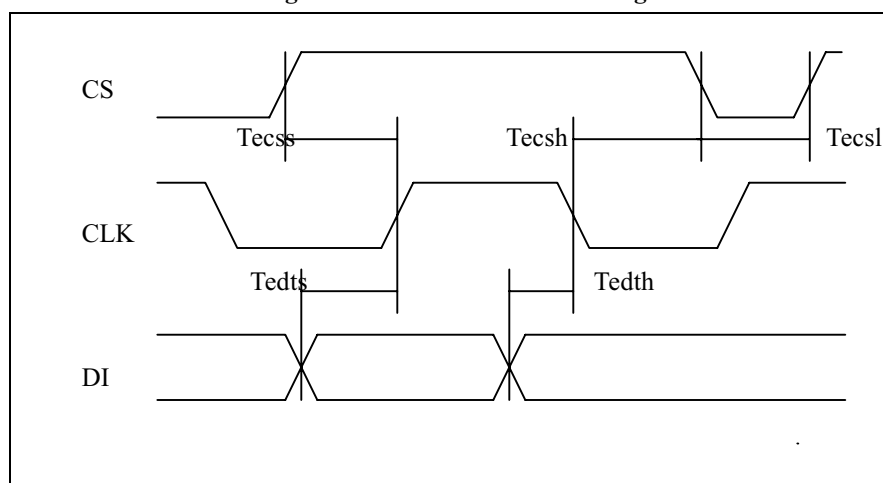
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| Parameter | Description | Condition | Min | Typical | Max | Units |
|-----------|-------------------------------|---------------|----------------|---------|---------------|-------|
| Tscf | Serial Clock Frequency | 2.7V<Vcc<5.5V | | | 0.4M/ 0.1M | Hz |
| Tecss | Delay from CS High to SK High | 2.7V<Vcc<5.5V | 160/640 | | | ns |
| Tecsh | Delay from SK Low to CS Low | 2.7V<Vcc<5.5V | 1120 /4480 | | | ns |
| Tedts | Setup Time of DI to SK | 2.7V<Vcc<5.5V | 160/640 | | | ns |
| Tedth | Hold Time of DI after SK | 2.7V<Vcc<5.5V | 2320 /9280 | | | ns |
| Tecsl | CS Low Time | 2.7V<Vcc<5.5V | 7400/ 29600 | | | ns |

Figure 17 Serial EEPROM timing**ADMtek Inc.**

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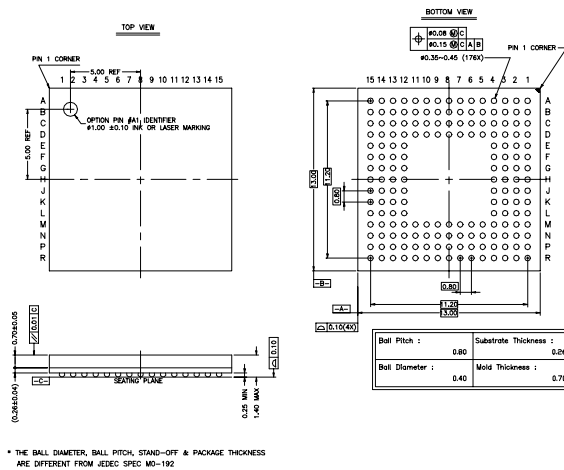
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ADM 9511

LAN/Modem Controller with Embedded Fast Ethernet PHY

12. Package



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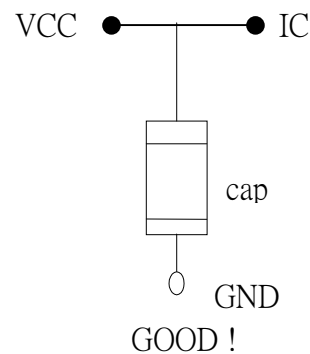
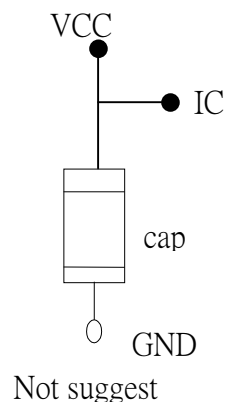
LAN/Modem Controller with Embedded Fast Ethernet PHY

Appendix 1 Layout Guide

Rev. 1.0B

1.placement

- a. Keep the distance as short as possible between ADM9511 and transformer, as well as transformer and RJ45.
- b. Make crystal device cross to ADM9511 pin x1 x2, and away from the following item:
 1. Tx+/- , Rx+/- differential pairs
 2. PCB edge.
 3. Transformer
 4. Any other high frequency components and associated traces.
- c. Pull-high resistor of Tx needs to close to chip and receiving termination resistor of Rx. capacitor needs to close to transformer.
- d. Decoupled capacitor should be placed as close to chip as possible and their traces should be as short as possible.
- e. Use ample dc-coupling and bulk capacitors to minimize noise.
- f. Use X7R ceramic capacitor for better capacitive characteristics over temperature.



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2.trace routing

a.Arrangement Tx and Rx trace

@Tx+/- and Rx+/- trace avoid right angle signal trace,suggest round angle >90°

Bad

Good



@Trace width must be wide that should be 2 times default value of layout software minimum request or wider than 8 miles.

@Signal trace length between Tx+/- differential pairs should be cross to equal length the total should no longer than 2 cm.The same requirement applies to Rx+/-.

@Make Tx and Rx trace route at the same signal plane and had better not using vias.

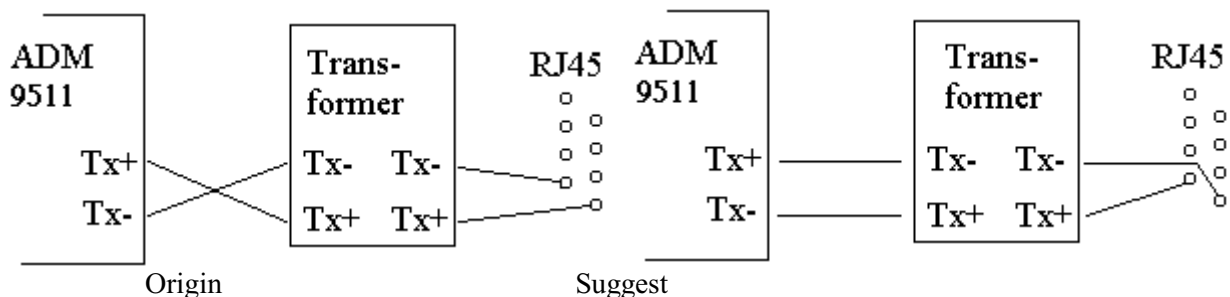
@Every differential pairs as cross as possible, but no less than 8 miles and the space should be almost equal .

@Keep the distance between the Tx and Rx differential pairs large, even separated ground planes underneath Tx and Rx signal pairs.

@Away from clock and power trace.

@If possible, with GND plane around.

@If Tx rount trace must cross, it should be swapped between chip and transformer.Transformor to RJ45 is also ,too.



@The high frequency signal trace width is 10~12mil.

@PCI clk signal trace length must be equal 2.5inch and other PCI bus signal trace length should be less than 1.5 inch

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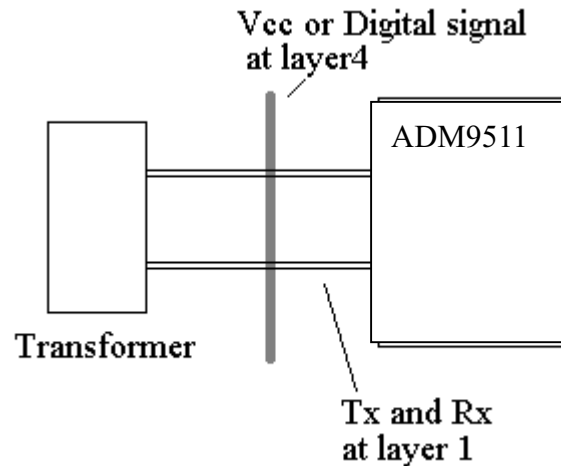
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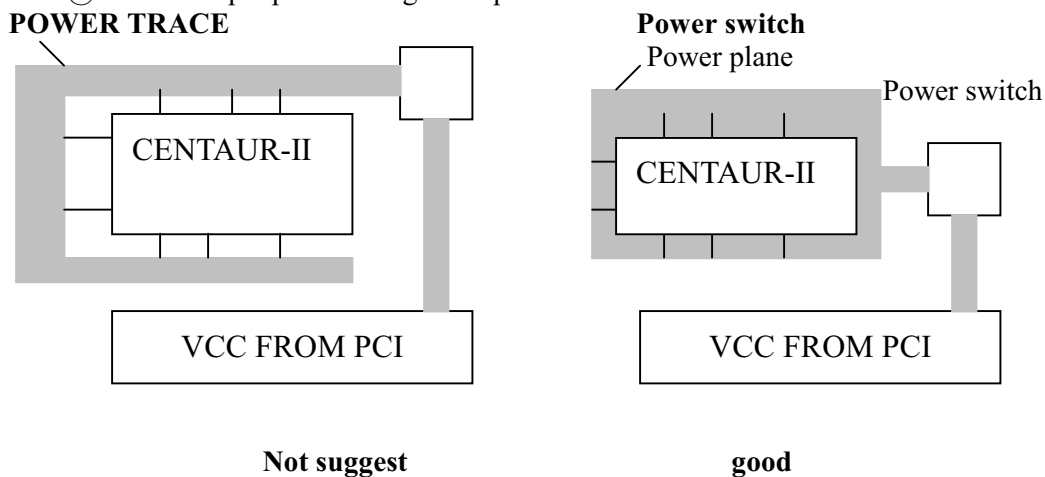
- b. Digital signal should be away from analog signal and power trace. If it can't be avoided, it is better to be crossed by 90 degrees with analog/Vcc routing at other planes.
- c. Vcc trace should be short and prefer to route in the format of the plane with a special for GND.

3. Vcc and GND



a. Vcc power:

- @ Avoid unnecessary trace being Vcc to IC and devices. keep these traces short and wide.
- @ Power trace width > 40 mils (if power trace route to the other side. It must use several via to connect each other).
- @ Power source use bulk capacitors (22~47uf) to reduce noise.
- @ Provide ample power and ground planes



c. GND plane

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@It is a good idea to fill in unused areas of signal planes with solid copper

@The signal ground region should be one continuous ,unbroken plane extending from the transformer through the rest of the board.

@On right angle is recommend when partition the Vcc and GND planes.

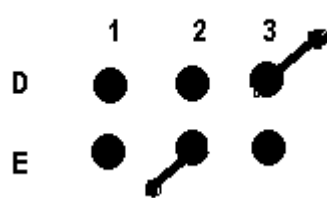
@For EMI consideration, add 0.1uF ceramic capacitors between system GND and chassis GND.

@Void the power and ground planes directly underneath the transformer and Pctel 303D/W circuit.

@The isolation voltage of the transformer should be rated to be greater than 2kv.

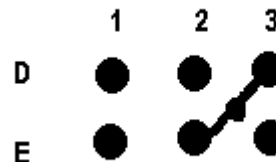
@There is an example of Vcc and GND planes below.

@ADM9511 pin E2 and pin D3 connect together first then connect to GND



Different GND via

Bad



use signal GND via

Good

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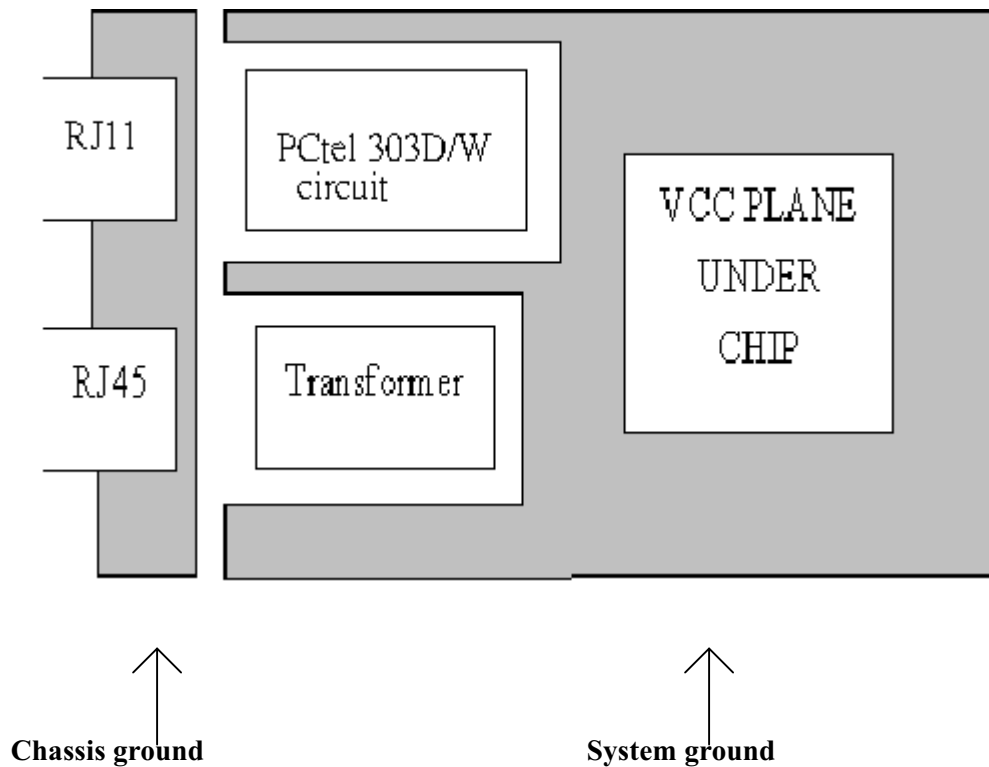
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ADM 9511**LAN/Modem Controller with Embedded Fast Ethernet PHY****4. Software modem layout guide**

Please reference Pctel demo board schematic , this schematic also include layout guide in it .

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