

2SJ550(L),2SJ550(S)

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

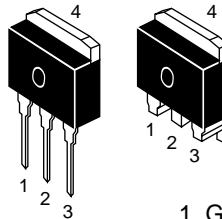
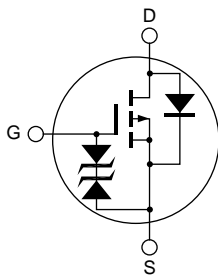
ADE-208-633A (Z)
2nd. Edition
Jun 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.075\Omega$ typ.
- Low drive current.
- 4V gate drive devices.
- High speed switching.

Outline

LDBPAK



1. Gate
2. Drain
3. Source
4. Drain

2SJ550(L),2SJ550(S)

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	-15	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	-60	A
Body-drain diode reverse drain current	I_{DR}	-15	A
Avalanche current	I_{AP} ^{Note3}	-15	A
Avalanche energy	E_{AR} ^{Note3}	19	mJ
Channel dissipation	P_{ch} ^{Note2}	50	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

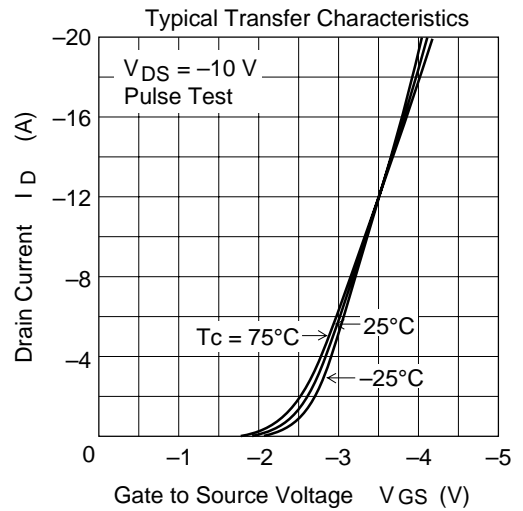
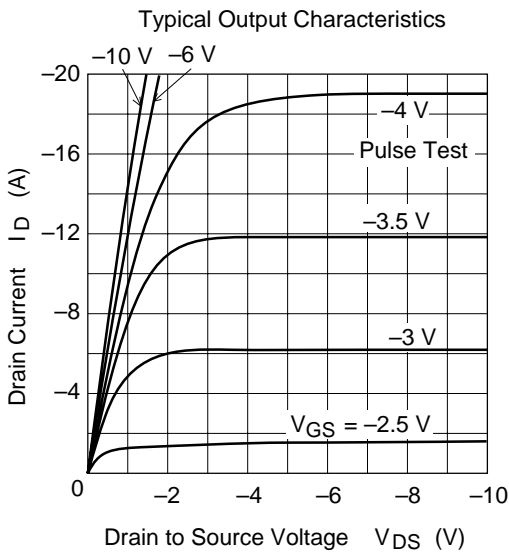
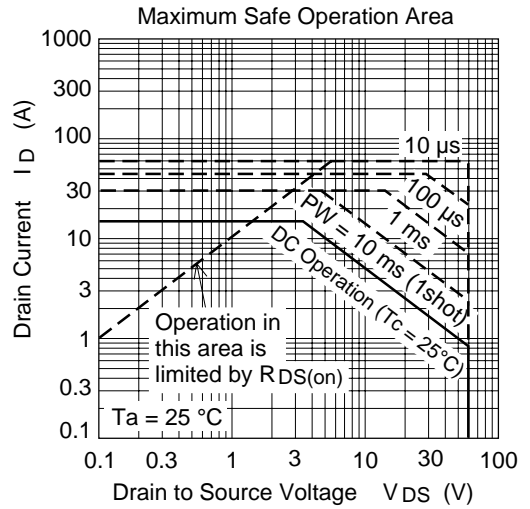
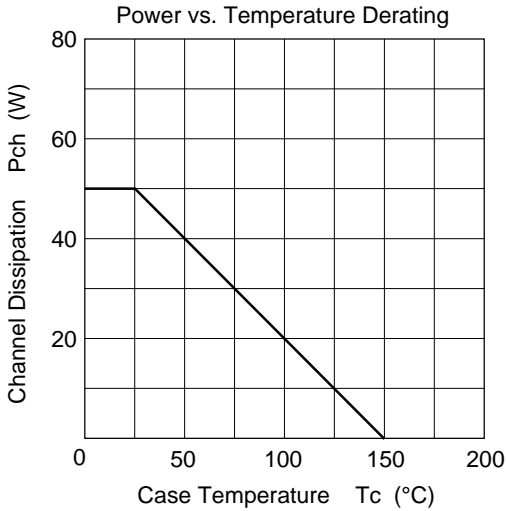
Note: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$
 2. Value at $T_c = 25^\circ C$
 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

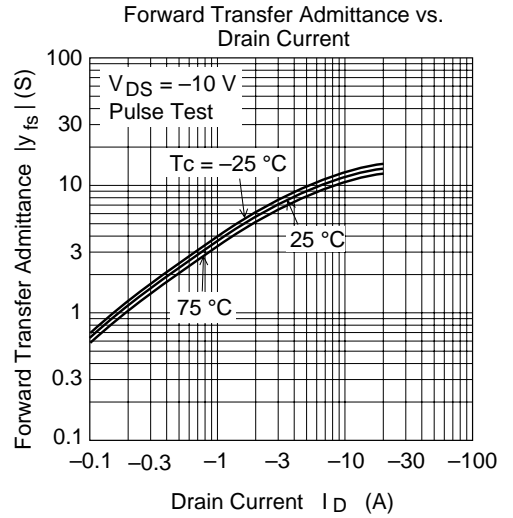
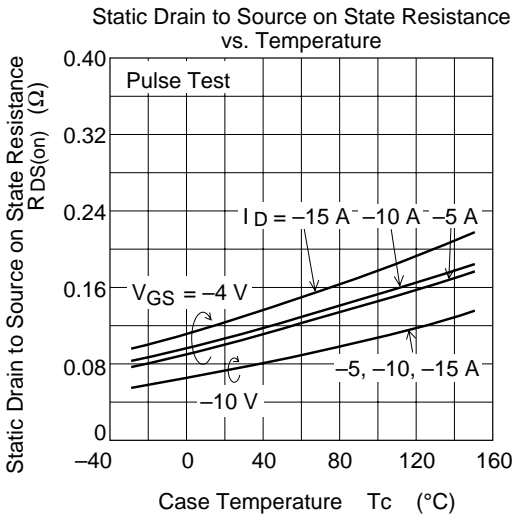
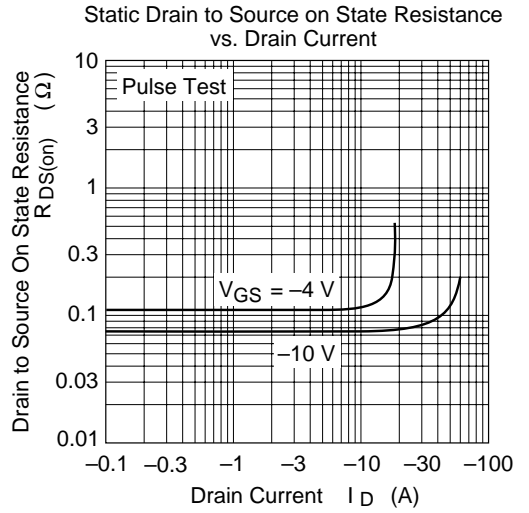
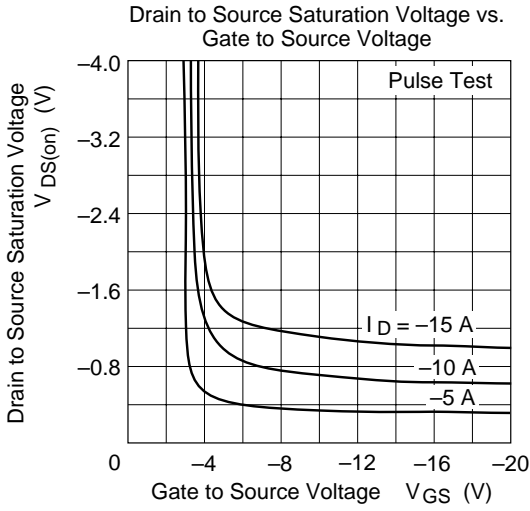
Electrical Characteristics (Ta = 25°C)

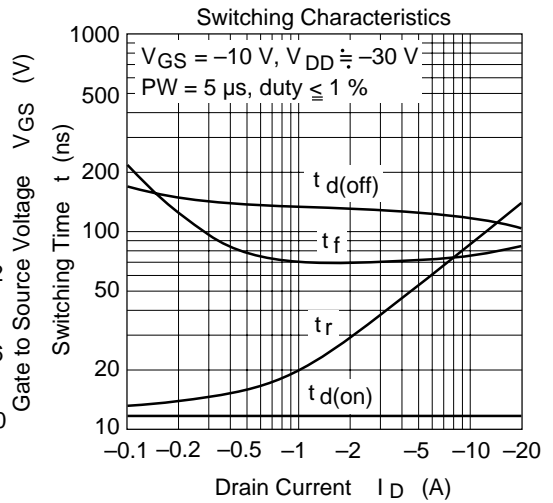
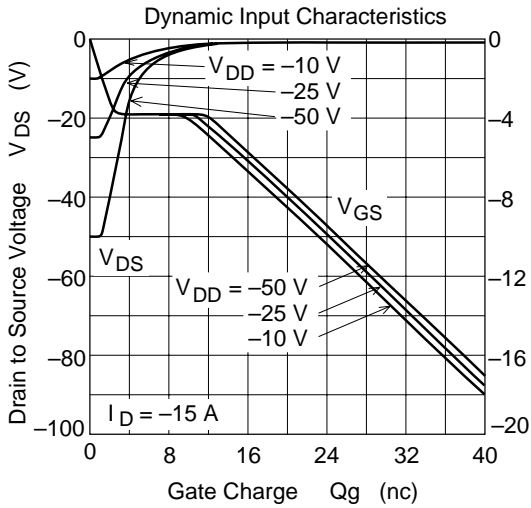
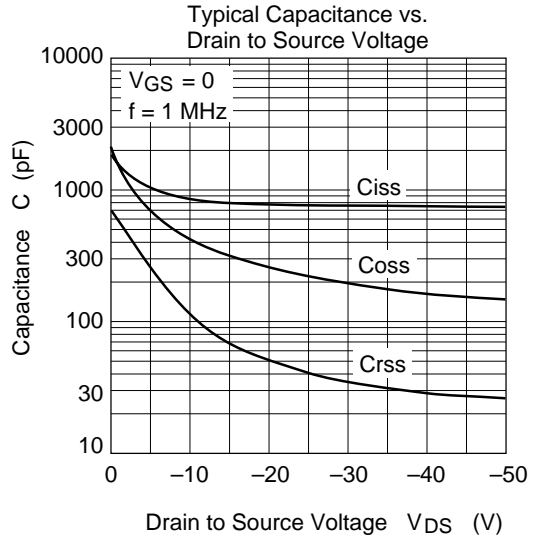
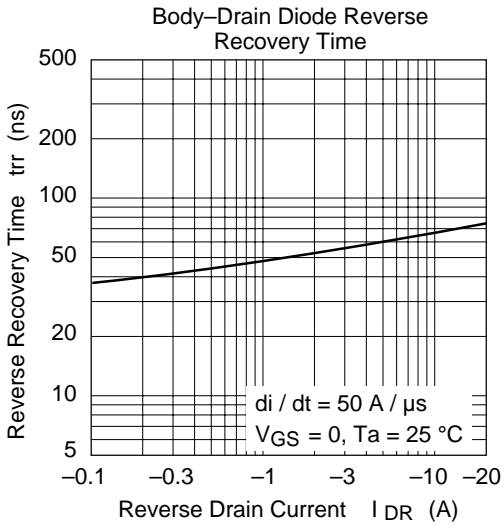
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10mA$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu A$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60V$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16V$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1mA$, $V_{DS} = -10V$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.075	0.095	Ω	$I_D = -8A$, $V_{GS} = -10V$ ^{Note4}
	$R_{DS(on)}$	—	0.105	0.155	Ω	$I_D = -8A$, $V_{GS} = -4V$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	6.5	11	—	S	$I_D = -8A$, $V_{DS} = -10V$ ^{Note4}
Input capacitance	C_{iss}	—	850	—	pF	$V_{DS} = -10V$
Output capacitance	C_{oss}	—	420	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	110	—	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = -10V$, $I_D = -8A$
Rise time	t_r	—	75	—	ns	$R_L = 3.75\Omega$
Turn-off delay time	$t_{d(off)}$	—	125	—	ns	
Fall time	t_f	—	75	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.1	—	V	$I_F = -15A$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = -15A$, $V_{GS} = 0$ $di_F/dt = 50A/\mu s$

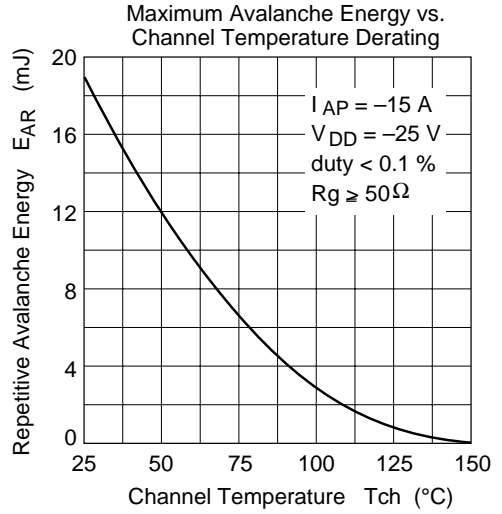
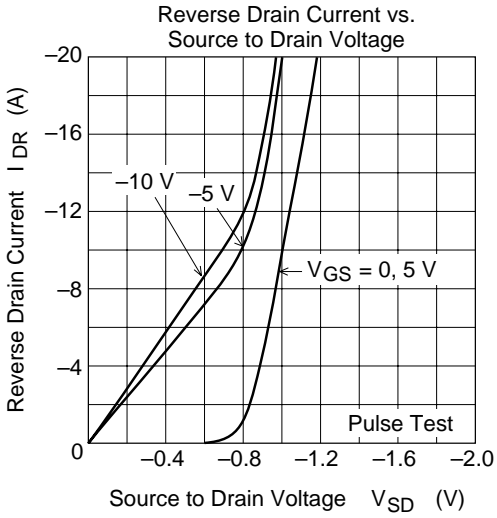
Note: 4. Pulse test

Main Characteristics

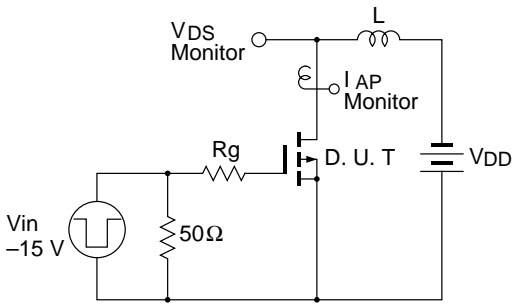






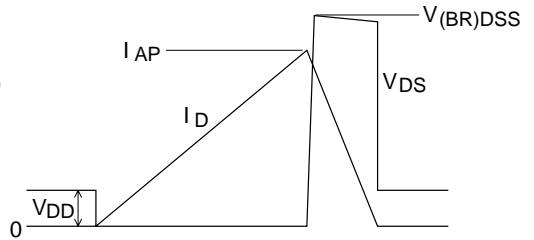


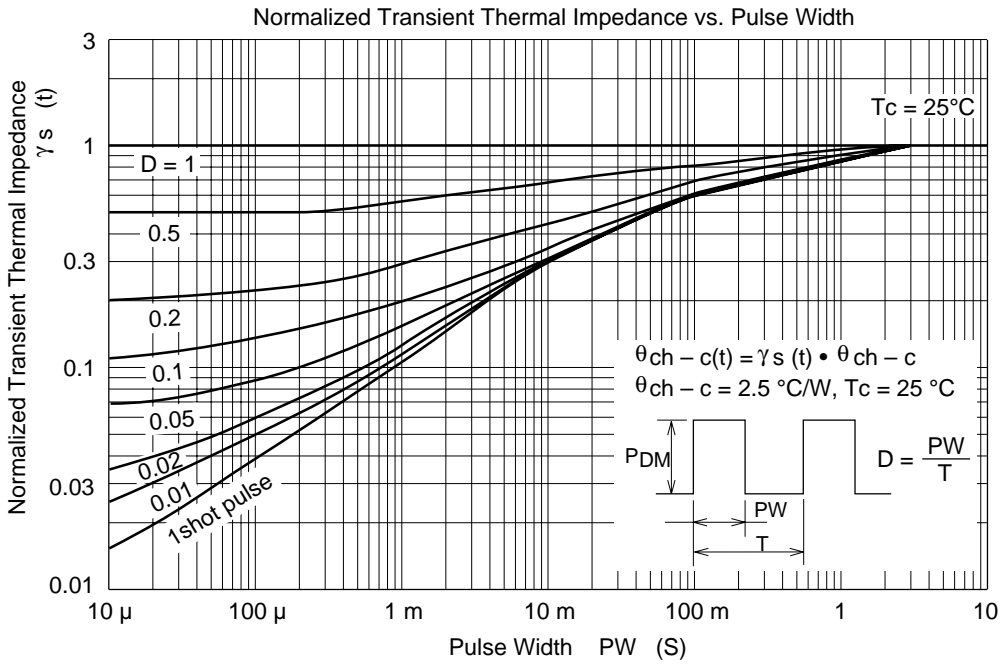
Avalanche Test Circuit



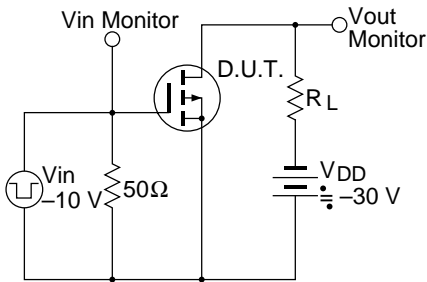
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

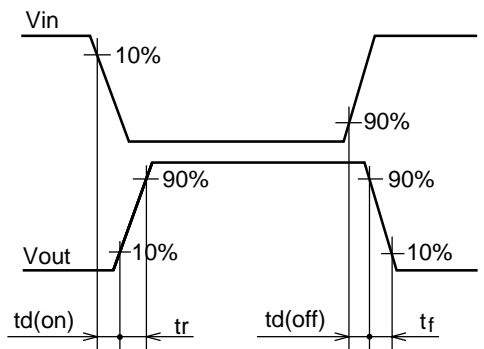




Switching Time Test Circuit

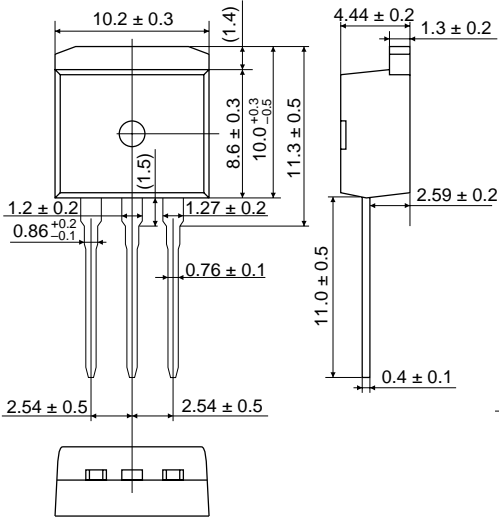


Waveform

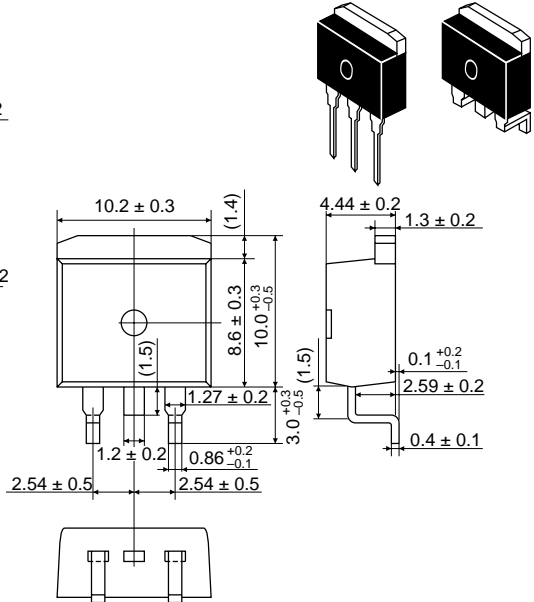


Package Dimensions

Unit: mm



Ⓛ type



Ⓢ type

Hitachi Code	LDBAK
EIAJ	—
JEDEC	—

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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