

2SJ496

Silicon P-Channel MOS FET
High Speed Power Switching

HITACHI

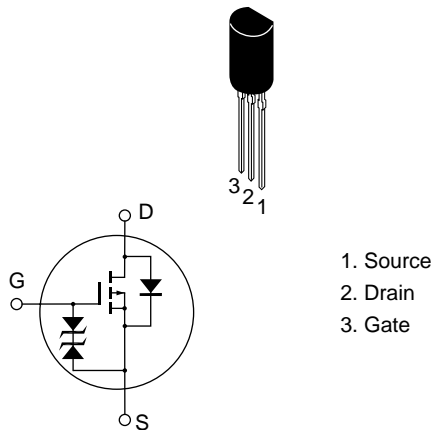
ADE-208-482
1st. Edition

Features

- Low on-resistance
 $R_{DS(on)} = 0.12\Omega$ typ. (at $V_{GS} = -10$ V, $I_D = -2.5$ A)
- 4V gate drive devices.
- Large current capacitance
 $I_D = -5$ A

Outline

TO-92 Mod



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-5	A
Drain peak current	$I_{D(pulse)}^{*1}$	-20	A
Body to drain diode reverse drain current	I_{DR}	-5	A
Avalanche current	I_{AP}^{*3}	-5	A
Avalanche energy	E_{AR}^{*3}	2.14	mJ
Channel dissipation	Pch^{*2}	0.9	W
Channel temperature	Tch	150	$^\circ\text{C}$
Storage temperature	Tstg	-55 to +150	$^\circ\text{C}$

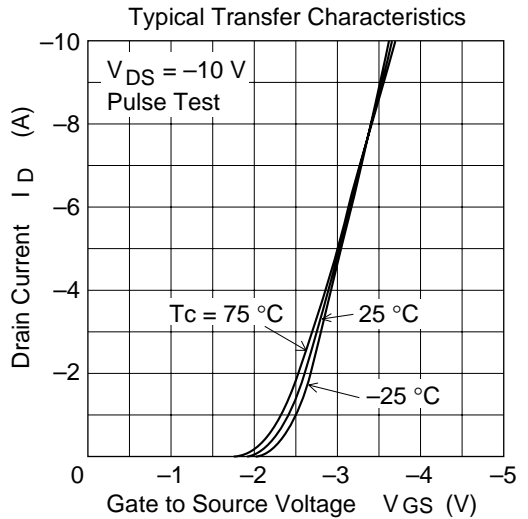
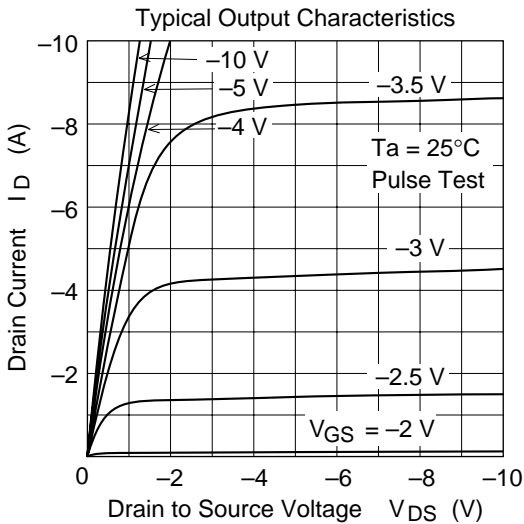
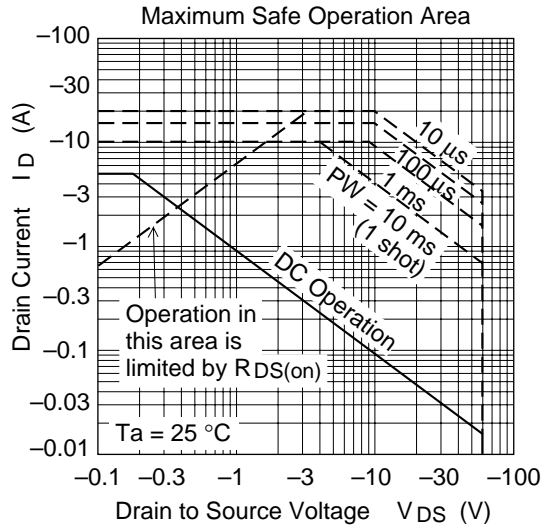
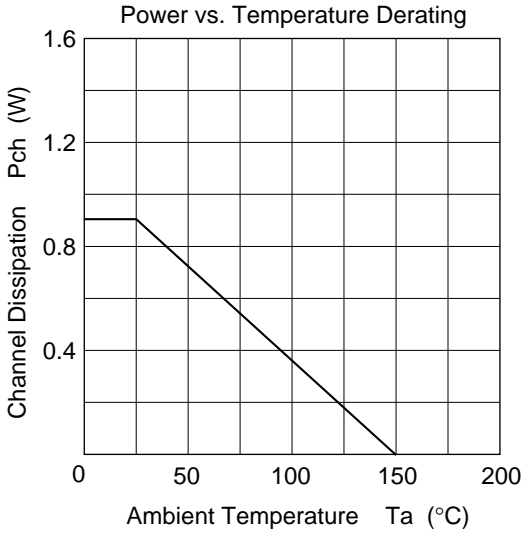
- Notes: 1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_a = 25^\circ\text{C}$
3. Value at $Tch = 25^\circ\text{C}$, $Rg \geq 50\ \Omega$

Electrical Characteristics (Ta = 25°C)

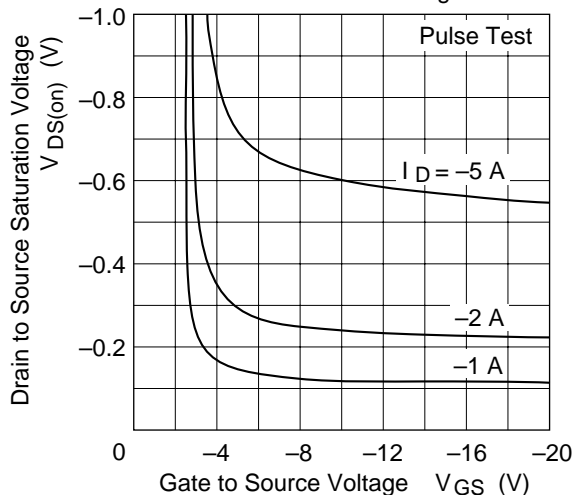
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.12	0.16	Ω	$I_D = -2.5\text{A}$ $V_{GS} = -10\text{V}^{*1}$
	$R_{DS(on)}$	—	0.17	0.24	Ω	$I_D = -2.5\text{A}$ $V_{GS} = -4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	3	5	—	S	$I_D = 2.5\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	C_{iss}	—	600	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	290	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	80	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$V_{GS} = -10\text{V}$, $I_D = -2.5\text{A}$
Rise time	t_r	—	25	—	ns	$R_L = 12\Omega$
Turn-off delay time	$t_{d(off)}$	—	95	—	ns	
Fall time	t_f	—	55	—	ns	
Body to drain diode forward voltage	V_{DF}	—	-1.0	—	V	$I_D = -5\text{A}$, $V_{GS} = 0$
Body to drain diode reverse recovery time	t_{rr}	—	65	—	ns	$I_F = -5\text{A}$, $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

Note: 1. Pulse test

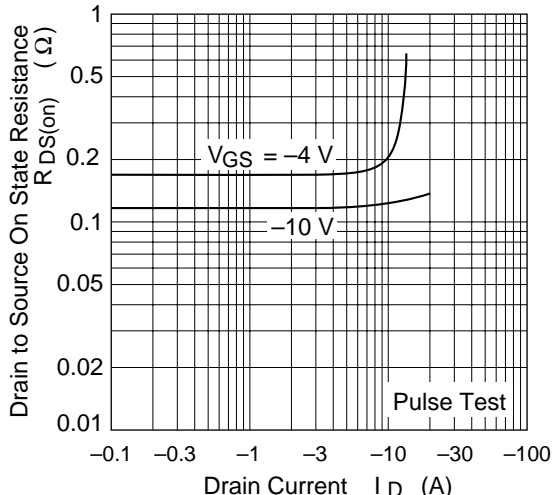
Main Characteristics



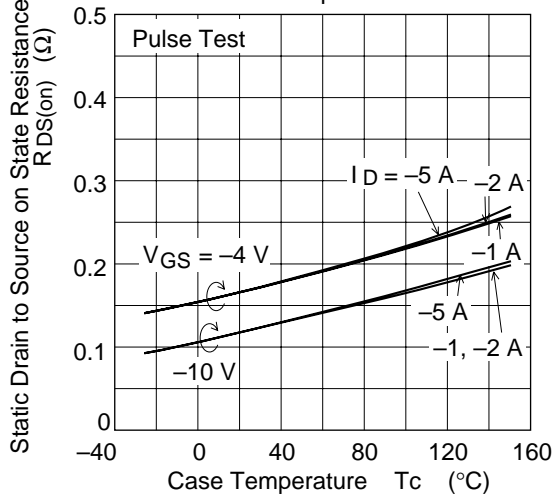
Drain to Source Saturation Voltage vs. Gate to Source Voltage



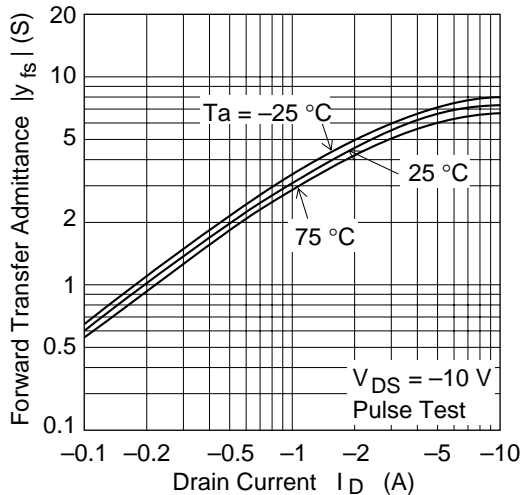
Static Drain to Source on State Resistance vs. Drain Current



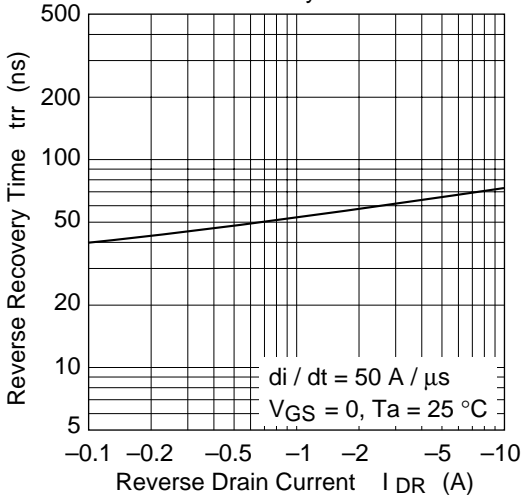
Static Drain to Source on State Resistance vs. Temperature



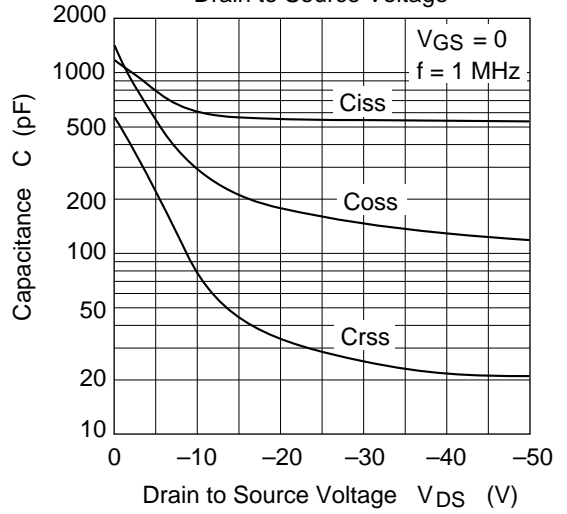
Forward Transfer Admittance vs. Drain Current



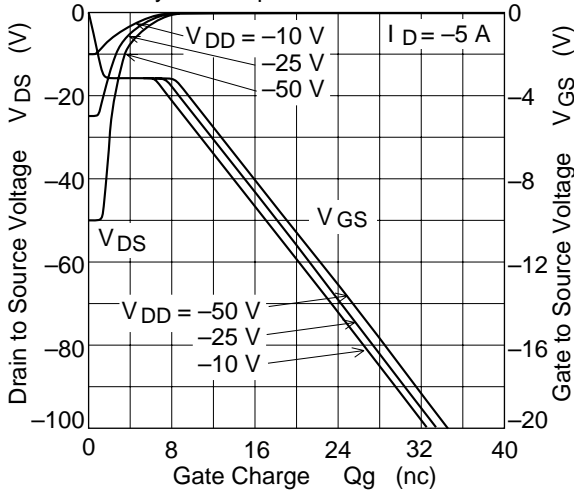
Body to Drain Diode Reverse Recovery Time



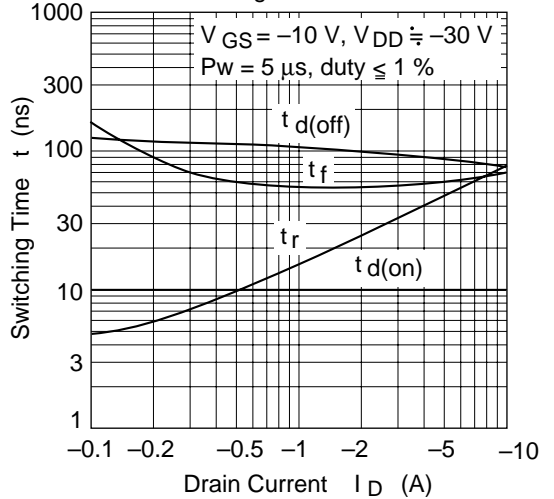
Typical Capacitance vs. Drain to Source Voltage



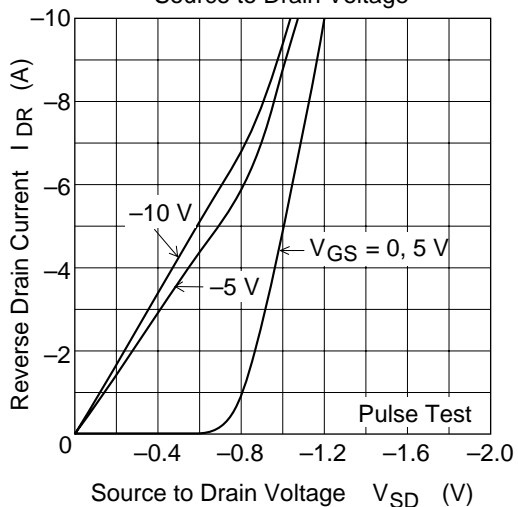
Dynamic Input Characteristics



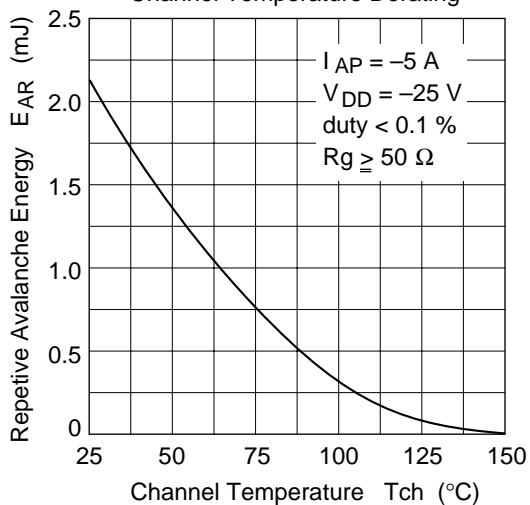
Switching Characteristics



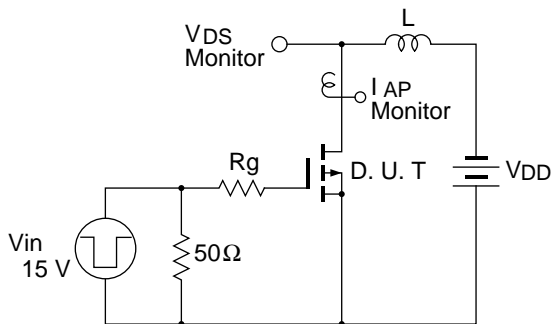
Reverse Drain Current vs. Source to Drain Voltage



Maximum Avalanche Energy vs. Channel Temperature Derating

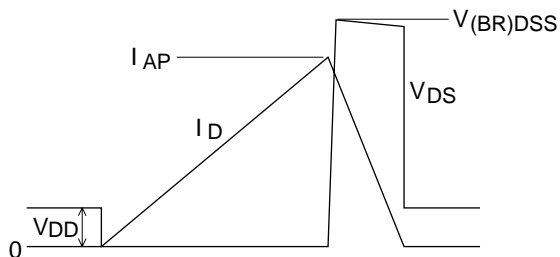


Avalanche Test Circuit

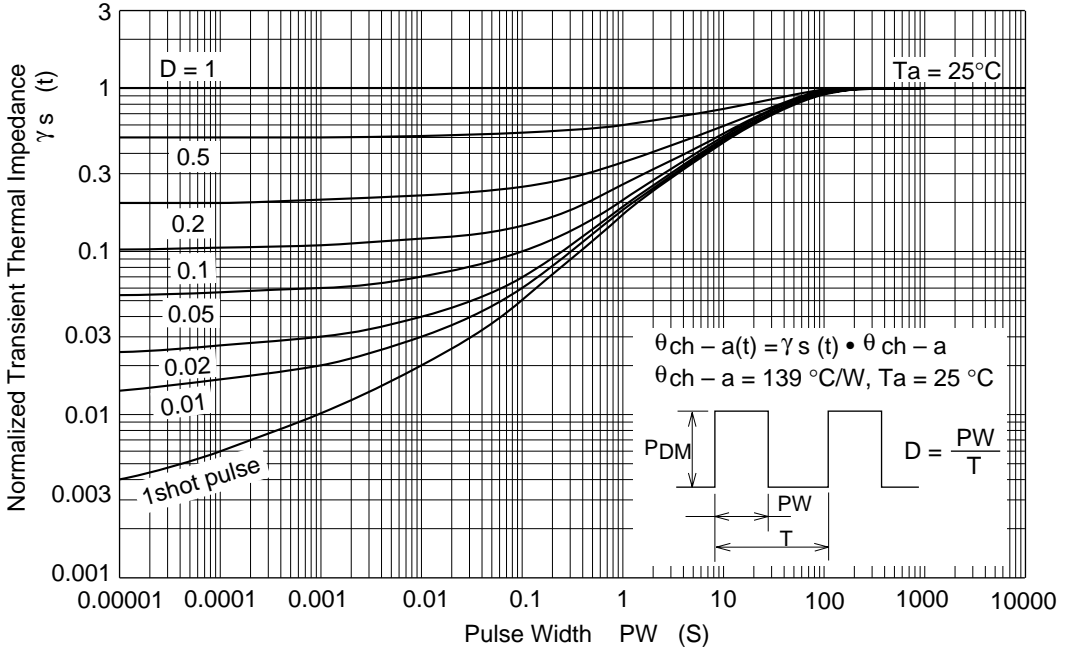


Avalanche Waveform

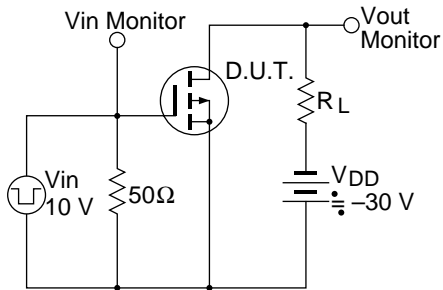
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



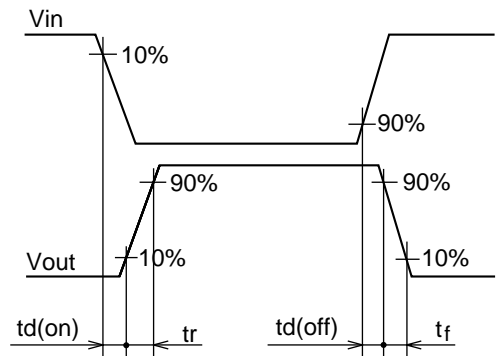
Normalized Transient Thermal Impedance vs. Pulse Width



Switching Time Test Circuit

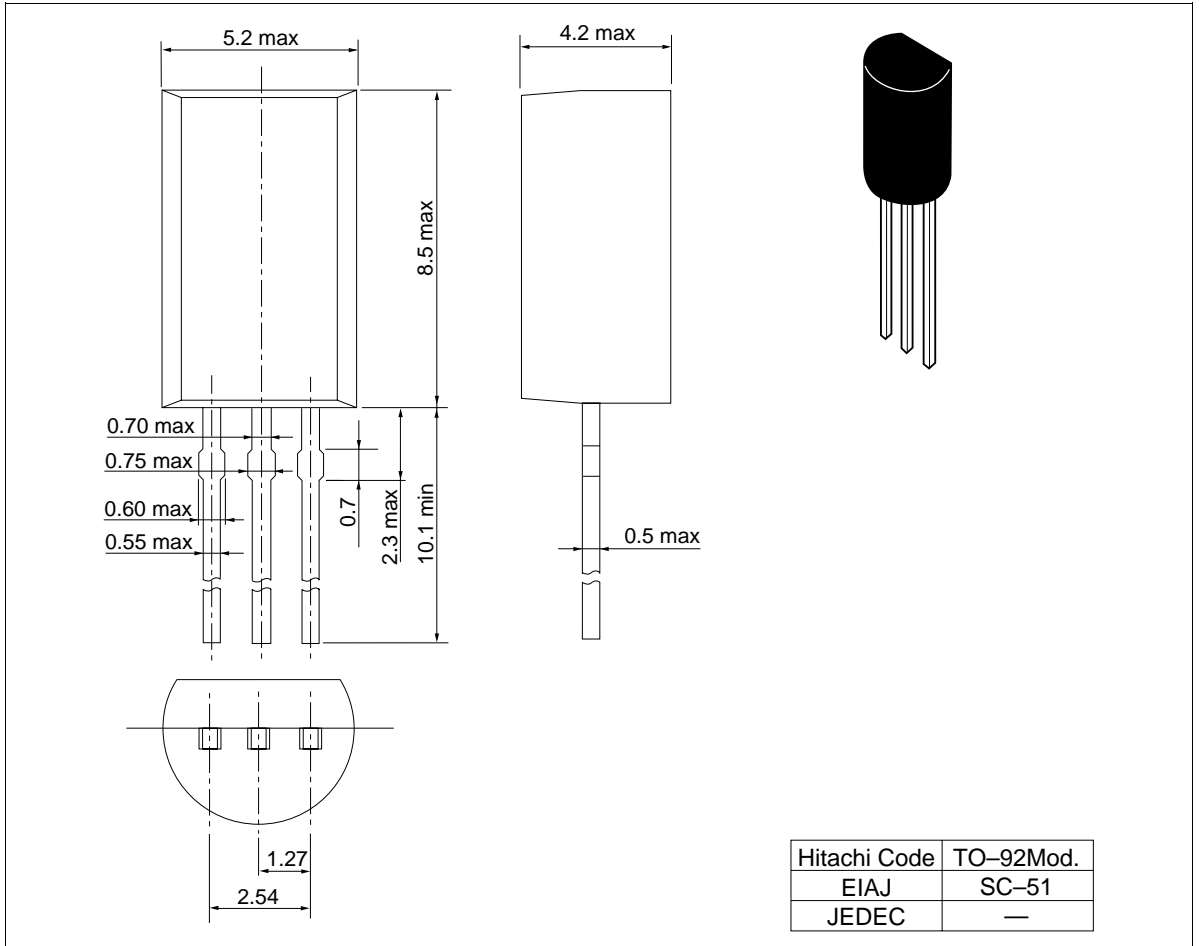


Switching Time Waveforms



Package Dimensions

Unit: mm



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