# NEC
## NEC Electronics Inc.

# µPD82C43
# CMOS INPUT/OUTPUT EXPANDER
# FOR µPD8048/C48 FAMILY

## Description

The µPD82C43 input/output expander is directly compatible with the µPD8048/C48 family of single-chip microcomputers. Using CMOS technology, the µPD82C43 provides high drive capabilities while requiring only a single +5 V supply voltage.

The µPD82C43 interfaces to the µPD8048/C48 family through a 4-bit I/O port and offers four 4-bit bidirectional static I/O ports. The ease of expansion allows for multiple µPD82C43s to be added using the bus port.

The bidirectional I/O ports of the µPD82C43 act as an extension of the I/O capabilities of the µPD8048/C48 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

## Features

- ☐ Four 4-bit I/O ports
- ☐ High output drive
- ☐ Logical AND and OR directly to ports
- ☐ Compatible with industry standard 8243
- ☐ Direct extension of resident µPD8048/C48 I/O ports
- ☐ Fully compatible with µPD8048/C48 microcomputer family
- ☐ CMOS technology
- ☐ Single +5 V supply

## Ordering Information

| Part Number | Package Type |
|---|---|
| µPD82C43C | 24-pin plastic DIP |
| µPD82C43CX | 24-pin plastic skinny DIP |

## Pin Configuration
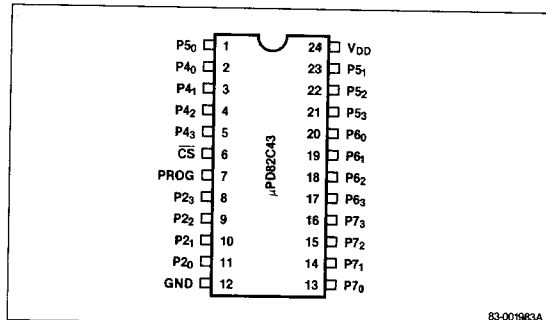


## Pin Identification

| No. | Symbol | Function |
|---|---|---|
| 1, 23–21 | $P5_0$–$P5_3$ | 4-bit I/O port 5 |
| 2–5 | $P4_0$–$P4_3$ | 4-bit I/O port 4 |
| 6 | $\overline{CS}$ | Chip select input |
| 7 | PROG | Clock input |
| 8–11 | $P2_3$–$P2_0$ | 4-bit I/O CPU interface port 2 |
| 12 | GND | Ground |
| 13–16 | $P7_0$–$P7_3$ | 4-bit I/O port 7 |
| 17–20 | $P6_3$–$P6_0$ | 4-bit I/O port 6 |
| 24 | $V_{DD}$ | +5 V power supply |

## Pin Functions

### $P2_0$-$P2_3$ (Port 2)

A 4-bit bidirectional port which contains the I/O port address and instruction code on a high to low transition of PROG. During a low to high transition of PROG, port 2 contains either the data for a selected output port if a write operation, or the data from a selected output port (before a low to high transition) if a read operation. Data on port 2 may be directly written, read, ANDed or ORed with previous data.

### $P4_0$-$P4_3$ (Port 4)

A 4-bit I/O port. May be programmed for input (during read), low impedance latched output (after write), or high impedance (after read).

### $P5_0$-$P5_3$ (Port 5)

A 4-bit I/O port. May be programmed for input (during read), low impedance latched output (after write), or high impedance (after read).

## P6₀-P6₃ (Port 6)

A 4-bit I/O port. May be programmed for input (during read), low impedance latched output (after write), or high impedance (after read).

## P7₀-P7₃ (Port 7)

A 4-bit I/O port. May be programmed for input (during read), low impedance latched output (after write), or high impedance (after read).

## $\overline{CS}$ (Chip Select)

A chip select input. A high on $\overline{CS}$ inhibits any change of output or internal status.

## PROG (Clock Input)

A high to low transition on PROG indicates that the op-code and the addressed port information are available on port 2. A low to high transition indicates that data is available on port 2.
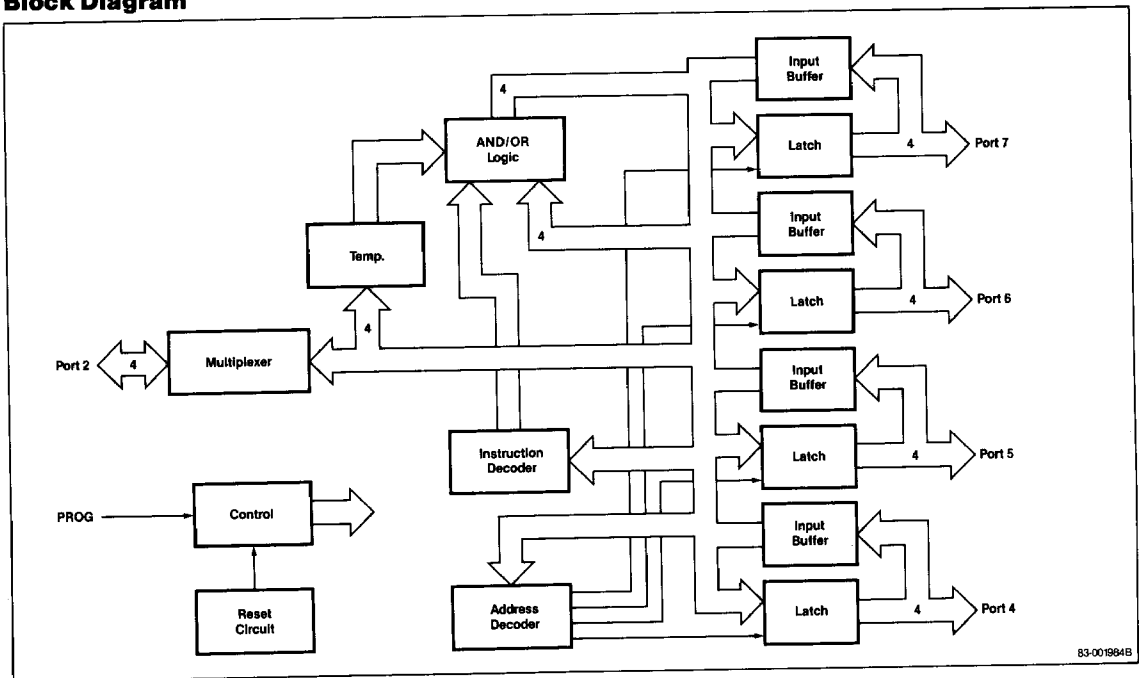
## Ground

Ground.

## V_DD (Power Supply)

+5 V power supply input.

## Block Diagram



83-001984B

## Absolute Maximum Ratings

$T_A = 25°C$

| | |
|---|---|
| Power supply voltage, $V_{DD}$ | $-0.5$ V to $+7$ V(1) |
| Input voltage, $V_I$ | $-0.3$ V to $V_{DD} +0.3$ V |
| Output voltage, $V_O$ | $-0.3$ V to $V_{DD} +0.3$ V |
| Operating temperature, $T_{OPT}$ | $-40°C$ to $+85°C$ |
| Storage temperature, $T_{STG}$ | $-65°C$ to $+150°C$ |
| Power dissipation, $P_D$ | 1.0 W |

**Note:**

(1) With respect to ground.

**Comment:** Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A = -40°C$ to $+85°C$; $V_{DD} = +5$ V $\pm 10\%$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input voltage high | $V_{IH}$ | $V_{DD} - 2.0$ | | $V_{DD}$ | V | |
| Input voltage low | $V_{IL}$ | $-0.3$ | | $+0.8$ | V | |
| Output voltage high (port 4–7) | $V_{OH1}$ | $V_{DD} - 0.5$ | | | V | $I_{OH} = -240 \mu A$ |
| Output voltage high (port 2) | $V_{OH2}$ | $V_{DD} - 0.5$ | | | V | $I_{OH} = -100 \mu A$ |
| Output voltage low (port 4–7) | $V_{OL1}$ | | | $+0.45$ | V | $I_{OL} = 5$ mA, (Note 1) |
| Output voltage low (port 7) | $V_{OL2}$ | | | $+1$ | V | $I_{OL} = +20$ mA |
| Output voltage low (port 2) | $V_{OL3}$ | | | $+0.45$ | V | $I_{OL} = 0.6$ mA |
| Sum of all $I_{OL}$ from 16 outputs | $I_{OL}$ | | | 80 | mA | 5 mA each pin |
| Input leakage current (port 4–7) | $I_{IL1}$ | | | $\pm 1$ | $\mu A$ | $V_{IN} = V_{DD}$ to 0 V |
| Input leakage current (port 2, $\overline{CS}$, PROG) | $I_{IL2}$ | | | $\pm 1$ | $\mu A$ | $V_{IN} = V_{DD}$ to 0 V |
| $V_{DD}$ supply current | $I_{DD1}$ | | 100 | 300 | $\mu A$ | |
| Power down supply current | $I_{DD2}$ | | 1 | 10 | $\mu A$ | |

**Note:**

(1) Refer to graph of additional sink current drive.

## DC Characteristics (cont)

$T_A = -40°C$ to $+85°C$; $V_{DD} = +2.5$ V to $+6$ V

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Input voltage high | $V_{IH}$ | $0.7 V_{DD}$ | | $V_{DD}$ | V | |
| Input voltage low | $V_{IL}$ | $-0.3$ | | $+0.18 V_{DD}$ | V | |
| Output voltage high (port 4–7) | $V_{OH1}$ | $0.75 V_{DD}$ | | | V | $I_{OH} = -120 \mu A$ |
| Output voltage high (port 2) | $V_{OH2}$ | $0.75 V_{DD}$ | | | V | $I_{OH} = -50 \mu A$ |
| Output voltage low (port 4–7) | $V_{OL1}$ | | | $+0.45$ | V | $I_{OL} = +2.5$ mA |
| Output voltage low (port 7) | $V_{OL2}$ | | | $+1$ | V | $I_{OL} = +7$ mA |
| Output voltage low (port 2) | $V_{OL3}$ | | | $+0.45$ | V | $I_{OL} = +0.3$ mA |
| Output current low (port 4–7) | $I_{OL}$ | | | 40 | mA | $+2.5$ mA each pin |
| Input leakage current (port 4–7) | $I_{IL1}$ | | | $\pm 1$ | $\mu A$ | $V_{IN} = V_{DD}$ to 0 V |
| Input leakage current (port 2, $\overline{CS}$, PROG) | $I_{IL2}$ | | | $\pm 1$ | $\mu A$ | $V_{IN} = V_{DD}$ to 0 V |
| $V_{DD}$ supply current | $I_{DD1}$ | | 100 | 300 | $\mu A$ | Operation mode, (Note 1) |
| Power down supply current | $I_{DD2}$ | | 1 | 10 | $\mu A$ | Standby mode |

**Note:**

(1) $I_{OH} = 0 \mu A$, PROG pulse cycle $= 5 \mu s$ min.

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## AC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = +5V \pm 10\%$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Code valid before PROG | $t_A$ | 100 | | | ns | 80 pF load |
| Code valid after PROG | $t_B$ | 0 | | | ns | 20 pF load |
| Data valid before PROG | $t_C$ | 200 | | | ns | 80 pF load |
| Data valid after PROG | $t_D$ | 20 | | | ns | 20 pF load |
| Port 2 floating after PROG | $t_H$ | 0 | | 150 | ns | 20 pF load |
| PROG negative pulse width | $t_K$ | 700 | | | ns | |
| Ports 4–7 valid after PROG | $t_{PO}$ | | | 700 | ns | 100 pF load |
| Ports 4–7 valid before / after PROG | $t_{IP}$ | 100 | | | ns | |
| Port 2 valid after PROG | $t_{ACC}$ | 90 | | 650 | ns | 80 pF load |
| CS valid before / after PROG | $t_{CS}$ | 50 | | | ns | |
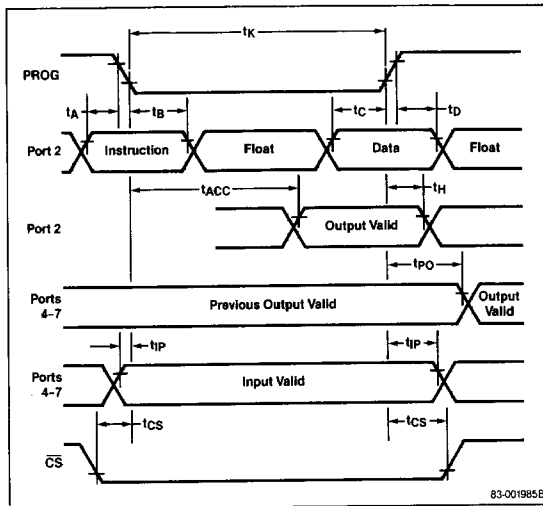
## AC Characteristics

$T_A = -40°C$ to $+85°C$, $V_{DD} = +2.5V$ to $+6V$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Command input setup time to PROG ↓ | $t_A$ | 300 | | | ns | Port 2 (control, port, address); 80 pF load |
| Command input setup time after PROG ↓ | $t_B$ | 0 | | | ns | Port 2 (control, port, address); 20 pF load |
| Data input setup time to PROG ↑ | $t_C$ | 600 | | | ns | Port 2 (write mode); 80 pF load |
| Data input hold time after PROG ↑ | $t_D$ | 80 | | | ns | Port 2 (write mode); 20 pF load |
| Data float delay time from PROG ↑ | $t_H$ | 0 | | 400 | ns | Port 2 (read mode); 20 pF load |
| PROG pulse width | $t_K$ | 2 | | | $\mu s$ | |
| CS input setup time to PROG ↓ CS input hold time after PROG ↑ | $t_{CS}$ | 200 | | | ns | |
| Data output delay time from PROG ↑ | $t_{PO}$ | | | 2 | ns | Port 4–7; 100 pF load |
| Data input setup time to PROG ↓ Data input hold time after PROG ↑ | $t_{IP}$ | 100 | | | ns | Port 4–7 |
| Data output delay time from PROG ↓ | $t_{ACC}$ | | | 3.5 | $\mu s$ | Port 2; 80 pF load |

## Timing Waveform



83-001985B

## Figure 1.    Current Sinking Capability (Note 1)



Maximum Sink Current at Any Pin [$V_{OL}$ = 0.4 V]
Maximum $I_{OL}$ Worst Cast Pin in mA

**Note:**

(1) This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD82C43 is capable of sinking 5 mA (for $V_{OL}$ = 0.4 V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

83-001986A

## Figure 2.    $t_{ACC}$ (Min)/μPD82C43 vs $t_{PC}$ (Max)/μPD80C48, μPD80C49



Frequency [MHz]

83-001987A
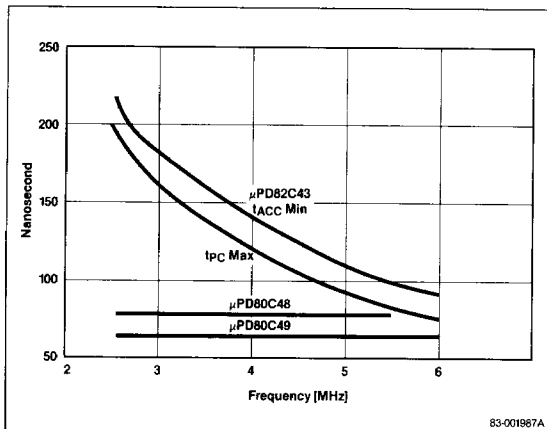
## Functional Description

The I/O capabilities of the μPD8048/C48 family can be enhanced in four I/O port increments of 4 bits each using one or more μPD82C43s. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND accumulator to port
- Logical OR accumulator to port
- Transfer port to accumulator
- Transfer accumulator to port

Port 2 ($P2_0$-$P2_3$) forms the 4-bit bus through which the μPD82C43 communicates with the host processor. The PROG output from the μPD8048/C48 family provides the necessary timing to the μPD82C43. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the opcode and port address followed by the second nibble containing the 4-bit data. Multiple μPD82C43s can be used for additional I/O. The output lines from the μPD8048/C48 family can be used to form the chip selects for additional μPD82C43s.

### Power On Initialization

Applying power to the μPD82C43 sets ports 4-7 to the high impedance mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high to low transition in order to exit from the power on mode. The power on sequence is initiated any time $V_{DD}$ drops below 1V. Table 1 following shows how the first 4-bit nibble of a data transfer instruction is decoded.

### Table 1.    Port 2 Instruction Decoding

| $P2_3$ | $P2_2$ | Instruction Code | $P2_1$ | $P2_0$ | Address Code |
|--------|--------|------------------|--------|--------|--------------|
| 0 | 0 | Read | 0 | 0 | Port 4 |
| 0 | 1 | Write | 0 | 1 | Port 5 |
| 1 | 0 | ORLD | 1 | 0 | Port 6 |
| 1 | 1 | ANLD | 1 | 1 | Port 7 |

For example, a 0010 appearing on $P2_3$-$P2_0$, respectively, would result in a read of port 6.

### Read Mode

There is one read mode in the μPD82C43. A falling edge on the PROG pin latches the op code and port address from input port 2. The port address and read operation are then decoded, causing the appropriate outputs to be high impedance and the input buffers switched on. The rising edge of PROG terminates the read operation. The port (4, 5, 6, or 7) that was selected by the port address ($P2_1$-$P2_0$) is returned to the high impedance mode, and port 2 is switched to the input mode.

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Generally, in the read mode a port will be an input and in the write mode it will be an output. If during program operation the μPD82C43's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

### Write Modes

There are three write modes in the μPD82C43. The MOVD $P_p$, A instruction from the μPD8048/C48 family writes the new data directly to the specified port (4, 5, 6,

or 7). The old data previously latched at that port is lost. The ORLD $P_p$, A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD $P_p$, A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.