NEC

MOS INTEGRATED CIRCUIT

μPD16655

240-OUTPUT TFT-LCD GATE DRIVER

The μPD16655 is a TFT-LCD gate driver equipped with 240-output lines. It can output a high-gate scanning voltage in response to 5 V/3.3 V CMOS level input because it provided with a level-shift circuit as a logic-input circuit. This gate driver is also provided with an output enable (OE) function, so that drivers can be installed at both sides.

FEATURES

- High-output voltage (V_{DD}-V_{EE} = amplitude: 31 V MAX.)
- Shift-direction select function
- Level shift of negative voltage V_{EE2}(level shift range: V_{DD}-V_{EE2} = 15 V)
- 5 V/3.3 V CMOS level interface
- Output enable function
- As many as 240-output lines
- Slim TCP

ORDERING INFORMATION

Part Number	Package
μPD16655N-xxx	TCP(TAB package)

Remark The TCP's external shape is custom model. To order your TCP's external shape, please contact a NEC salesperson.

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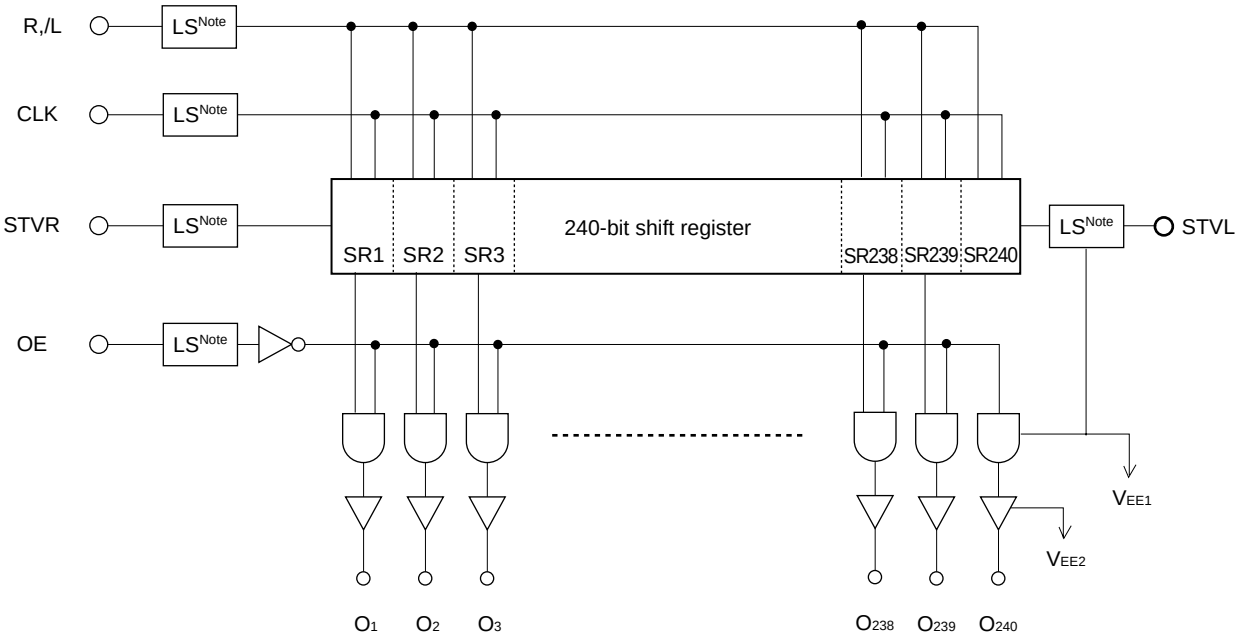
The mark ★ shows major revised points.

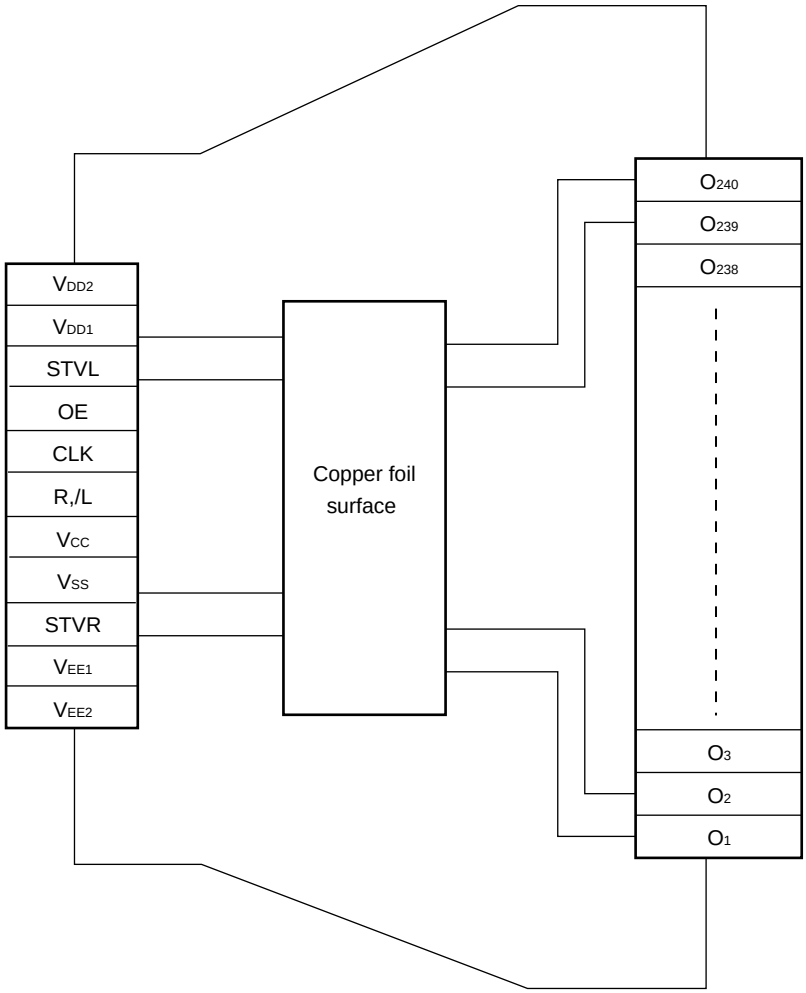
1. BLOCK DIAGRAM



Note LS (level shifter): Shifts 5 V/3.3 V CMOS level and V_{DD2}-V_{EE1} level.

Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μPD16655N-xxx)



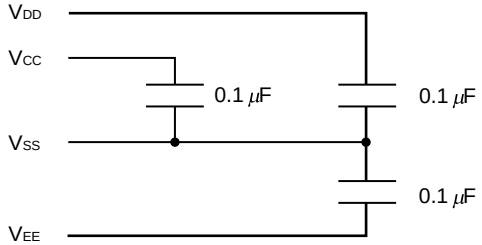
Remark This figure does not specify the TCP package.

★ 3. PIN FUNCTIONS

SYMBOL	PIN NAME	I/O	DESCRIPTION
O_1 to O_{240}	Driver Output		These pins output scan signals that drive the vertical direction (gate lines) of a TFT-LCD. The output signals change in synchronization with the rising edge of shift clock CLK. The driver output amplitude is V_{DD2} - V_{EE2}.
STVR STVL	Start Pulse Input/Output	V_{SS}/V_{CC} or V_{DD1}/V_{EE1} (input)	This is the input of the internal shift register. The input date is read at the rising edge of shift clock CLK, and scan signals are output from the O_1 through O_{120} pins. The input level is a V_{CC}/V_{SS} or V_{DD1} - V_{EE1} level.
		V_{DD1}/V_{EE1} (output)	This pin outputs a start pulse to the μPD16655 at the next stage when two or more μPD16655s are connected in cascade. The pulse is output at the falling edge of the 240th clock of shift clock CLK, and is cleared at the falling edge of the 241st clock.
R,/L	Shift Direction Select Input	V_{SS}/V_{CC} or V_{DD1}/V_{EE1}	R,/L = "H" (right shift): STVR → O_1 → O_{240} → STVL R,/L = "L" (left shift): STVL → O_{240} → O_1 → STVR
CLK	Shift Clock Input	V_{SS}/V_{CC}	This pin inputs a shift clock to the internal shift register. The shift operation is performed in synchronization with the rising edge of this input.
OE	Output Enable Input	V_{SS}/V_{CC}	When this pin goes "H", the driver output is fixed to "L". The shift register is not cleared, however. The internal logic operates even when OE = "H". OE is in asynchronization with the clock.
V_{DD1}	Logic Positive Power Supply		10 V to 25 V
V_{DD2}	Driver Positive Power Supply		10 V to 25 V
V_{CC}	Reference Positive Power Supply		3.0 to 5.5 V Reference voltage to level shifter LS.
V_{SS}	Reference Negative Power Supply		Connect this pin to the ground of the system.
V_{EE1}	Logic Negative Power Supply		–21 V to –3 V
V_{EE2}	Driver Negative Power Supply		–21 V to V_{DD2} – 15 V

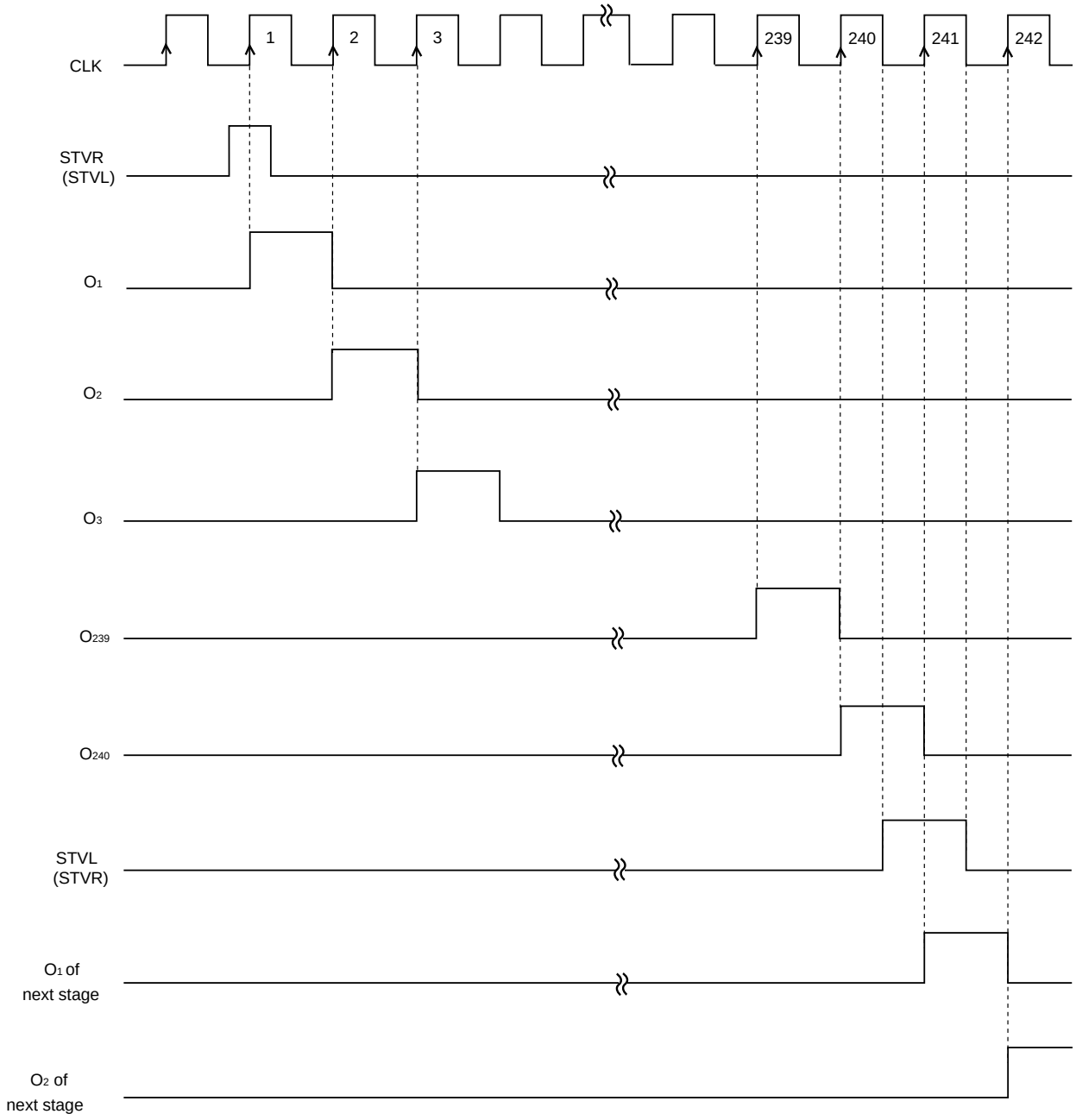
Cautions 1. To prevent latch up, turn on power to V_{CC}, V_{EE1}-V_{EE2}, V_{DD1}-V_{DD2}, and logic input in this order. Turn off power in the reverse order. These power up/down sequence must be observed also during transition period.

2. Insert a capacitor of about 0.1 μF between each power line, as shown below, to secure noise margin such as V_{IH} and V_{IL}, because the internal logic operates on a high voltage level. ($V_{DD} = V_{DD1} = V_{DD2}$)



3. **In an application where the V_{EE} power supply is not shifted, short-circuit V_{EE2} (driver power) and V_{EE1} (logic power) outside the TCP. Fix unused pins to the V_{EE} level.**
4. **The level shift range of V_{EE2} must be $V_{EE1} \leq V_{EE2} \leq V_{DD} - 15$ V. Note that, in this case, the guaranteed values of the output ON resistance and output fall time slightly change. ($V_{DD} = V_{DD1} = V_{DD2}$)**

5. TIMING CHART



Caution Do not use a sequence in which the outputs change all at once because such a sequence may cause malfunctioning.

★ 6. ELECTRICAL SPECIFICATION

Absolute Maximum Ratings (T_A = 25°C, V_{SS} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Positive Supply Voltage	V_{DD1}	–0.5 to +28	V
Driver Positive Supply Voltage	V_{DD2}	–0.5 to +28	V
Reference Positive Power Supply Voltage	V_{CC}	–0.5 to +7	V
Power Supply Voltage	V_{DD1}-V_{EE1} V_{DD2}-V_{EE2}	–0.5 to +33	V
Logic Negative Supply Voltage	V_{EE1}	–23 to +0.5	V
Driver Negative Supply Voltage	V_{EE2}	–23 to +0.5	V
Input Voltage	V_I	V_{EE1} – 0.5 to V_{DD1} + 0.5	V
Input Current	I_I	±10	mA
Output Current	I_O	±10	mA
Operating Temperature Range	T_A	–30 to +85	°C
Storage Temperature Range	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –30 to 85°C, V_{SS} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Positive Supply Voltage	V_{DD1}	10		25	V
Driver Positive Supply Voltage	V_{DD2}	10		25	V
Logic Negative Supply Voltage	V_{EE1}	–21		–3	V
Driver Negative Supply Voltage	V_{EE2}	–21		V_{DD2} – 15	V
Power Supply Voltage	V_{DD1}-V_{EE1} V_{DD2}-V_{EE2}	15		31	V
Reference Positive Power Supply Voltage	V_{CC}	2.7		5.5	V

Caution Observe the following condition when shifting V_{EE2} (driver power). Note that, in this case, the guaranteed values of the output ON resistance and output fall time slightly change.
$V_{EE1} \leq V_{EE2} \leq V_{DD}$ – 15 V (V_{DD1} or V_{DD2})

ELECTRICAL CHARACTERISTICS (T_A = –30 to +85 °C, V_{DD1} = V_{DD2} = 22 V, V_{EE1} = V_{EE2} = –9 V, V_{SS} = 0 V, V_{CC} = 2.7 V or 5.5 V)

Parameter	Symbol	Condition	MIN	TYP.	MAX.	Unit
High-Level Input Voltage	V_{IH}		0.7 V_{CC}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}		V_{EE1}		0.3 V_{CC}	V
High-Level Output Voltage	V_{OH}	STVR-STVL, without load	V_{DD1} – 0.05		V_{DD1}	V
Low-Level Output Voltage	V_{OL}	STVR-STVL, without load	V_{EE1}		V_{EE1} + 0.05	V
High-Level Output Driver Current	I_{XOH}	Driver output, V_O = V_{DD2} – 1.0 V			–2.0	mA
Low-Level Output Driver Current	I_{XOL1}	Driver output, V_O = V_{EE2} + 1.0 V	2.0			mA
	I_{XOL2}	Driver output, V_O = V_{EE2} + 1.0 V, V_{EE2} = V_{DD} – 15 V	1.5			mA
LCD Driver Output ON Resistance	R_{ON1}	V_O = V_{EE2} + 1.0 V, V_{DD2} – 1.0 V			500	Ω
	R_{ON2}	V_O = V_{EE2} + 1.0 V, V_{DD2} – 1.0 V, V_{EE2} = V_{DD} – 15 V			700	Ω
High-Level Output Pulse Current	I_{POH}	STVR-STVL, V_O = V_{DD1} – 1.0 V			–2.0	mA
Low-Level Output Pulse Current	I_{POL}	STVR-STVL, V_O = V_{EE1} + 1.0 V	2.0			mA
Input Leak Current	I_{IL}	V_I = 0 V or 3 V or 5 V			±1	μA
Static Current Dissipation	I_{DD}	V_{DD1}, V_{DD2} pin, f_{CLK} = 31.5 kHz		400	800	μA
	I_{EE}	V_{EE1}, V_{EE2} pin, f_{CLK} = 31.5 kHz		–400	–800	μA
	I_{CC}	V_{CC} pin, f_{CLK} = 31.5 kHz			50	μA

★ **SWICHING CHARACTERISTICS (T_A = –30 to +85 °C, V_{DD1} = V_{DD2} = 22 V, V_{EE1} = V_{EE2} = –9 V, V_{SS} = 0 V, V_{CC} = 2.7 V to 5.5 V)**

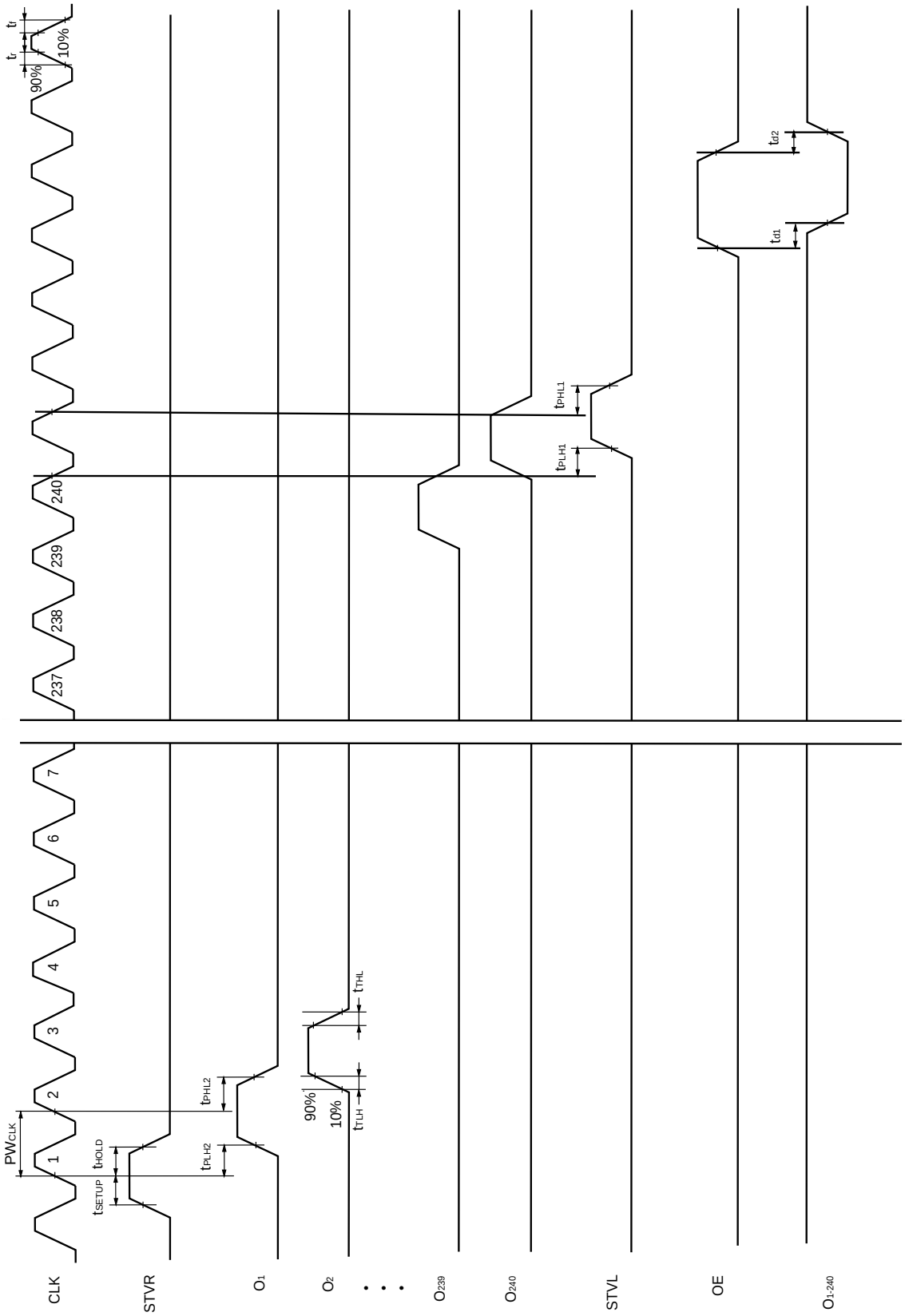
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cascade Output Delay Time	t_{PHL1}	C_L = 20 pF			600	ns
	t_{PLH1}				600	ns
Driver Output Delay Time	t_{PHL2}	C_L = 220 pF CLK → X_{on}			700	ns
	t_{PLH2}				700	ns
	t_{d1}	C_L = 220 pF, OE: L → H			700	ns
	t_{d2}	C_L = 220 pF, OE: H → L			700	ns
Output Rise Time	t_{TLH}	C_L = 220 pF			300	ns
Output Fall Time	t_{THL1}	C_L = 220 pF			300	ns
	t_{THL2}	C_L = 220 pF, V_{EE2} = V_{DD} – 15 V			400	ns
Input Capacitance	C_I	T_A = 25°C			15	pF
Clock Frequency	f_{CLK}	In cascade connection	100			kHz

★ **TIMING REQUIREMENTS (T_A = –30 to 85 °C, V_{DD1} = V_{DD2} = 22 V, V_{EE1} = V_{EE2} = –9 V, V_{SS} = 0 V, V_{CC} = 2.7 V to 5.5 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}		1000			ns
Data Setup Time	t_{setup}	STVR(STVL) ↑ → CLK ↑	100			ns
Data Hold Time	t_{hold}	CLK ↑ → STVR(STVL) ↓	100			ns

Caution Keep the time and fall time of the logic input to t_r = t_f = 20 ns (10 to 90 % of the rated values).

★ 7. SWITCHING CHARACTERISTIC WAVEFORM



8. RECOMMENDED SOLDERING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16655.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16655N-xxx : TCP(TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds: pressure 100 g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C; pressure 3 to 8 kg/cm^2; time 3 to 5 secs. Real bonding 165 to 180°C; pressure 25 to 45 kg/cm^2, time 30 to 40 secs. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd.)

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability / Quality Control System (C10983E)

Quality Grades to NEC's Semiconductor Devices (C11531E)

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